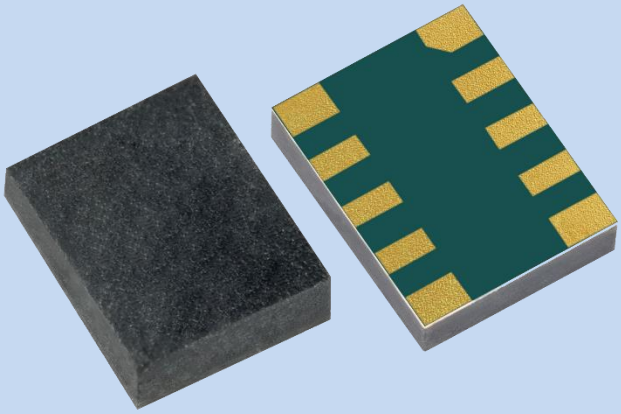


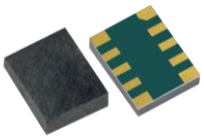
REAL TIME CLOCK MODULE

RTT21064

Rev C

RTT21064

Real Time Clock Oscillator

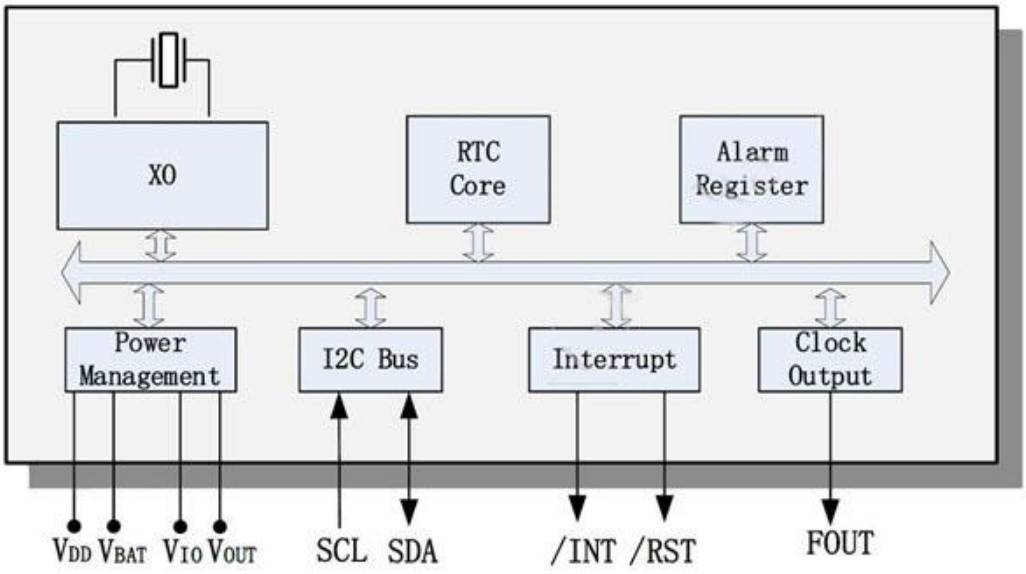


RTT21064 is an I2C bus interface real-time clock with low power consumption and digital offset function. It supports backup battery and embeds a 32.768KHz TCXO. It supports calendar (year, month, day, hour, minute, second), clock and timer functions etc. The SMD3225 package with only 1.0mm thickness makes it very suitable to be used in portable and small size electronic devices

KEY FEATURES

- Low current consumption: 1.0uA (Typ.)
- High stability: 5±23ppm max @ +25℃
- Build-in TCXO: 32.768kHz
- Communication interface: I2C bus
- Power supply voltage: 1.6V~5.5V
- Timekeeper voltage: 1.2V~5.5V
- Operation Temperature Range: -40℃ ~ +85℃
- Leap years autocorrection
- Timer output function with adjustable period
- Package: 3.2mm × 2.5mm × 1.0mm
- Digital offset function

BLOCK DIAGRAM



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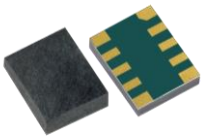


ELECTRICAL SPECIFICATIONS

1.1 Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Power supply voltage	V_{DD}		-0.3		6.5	V
Internal voltage	V_{OUT}		-0.3		6.5	V
Backup battery voltage	V_{BAT}		-0.3		6.5	V
Interface voltage	V_{IO}		-0.3		6.5	V
Input voltage	V_{IN}	SCL, SDA input	GND-0.3		6.5	V
Clock output voltage	V_{OUT1}	FOUT output	GND-0.3		V_{DD}+0.3	V
Output voltage	V_{OUT2}	SDA, /INT output	GND-0.3		6.5	V
Storage temperature	T_{STG}		-55		125	℃

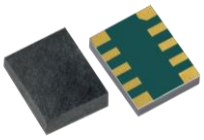
1.2 Recommended Operating Conditions

Table 2. Recommended Operating Conditions

Unless otherwise specified, GND=0V, Ta=40℃~+85℃

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Power Supply Voltage (normal mode)	V_{DD}		1.25	3.0	5.5	V
Interface voltage	V_{IO}	VDD=VDET1~5.5V When VDD becomes less than VDET1, the interface will halt.	1.6	3.0	5.5	V
Backup Battery	V_{BAT}		1.2	3.0	5.5	V
Current consumption	I_{DD}	Using Battery supply		1.0		uA
Operation temperature	T_{OPR}		-40	25	85	℃

Note 1: To apply min. value of V_{DD} and V_{BAT}, V_{DD} and V_{BAT} need to be supplied with more than 1.5V at least for the oscillation to stabilize (oscillation start time t_{STA}).



1.3 Frequency Characteristics

Table 3. Frequency Characteristics

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Frequency Accuracy	Δf/f	VDD=3.0V; @+25℃	5±23			ppm
Frequency Stability	Δf2/f	VDD=3.0V ; -20℃ ~ +70℃; Reference frequency @ +25℃	-120		±10	ppm
Oscillation Start Time	tSTA				1	s
Year Aging	fa				±5	ppm
FOUT duty cycle	tw/t		40	50	60	%

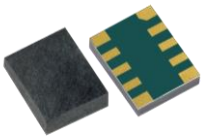
Unless otherwise specified, GND=0V, Ta=40℃~+85℃

1.4 DC Characteristics

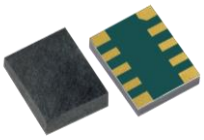
Table 4. DC Characteristics

Unless otherwise specified, GND=0V, V_{BAT}=V_{DD}=1.2~5.5V, V_{IO}=1.6V ~5.5V, Ta=40℃~+85℃

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Average Current consumption1	IDD1	SCL=SDA = 'H', FOUT=OFF, /IRQ=OFF, VDD=VIO=3.0V,CHGEN=0b or VBAT≧ VDET3, -40℃~85℃		1.0	5.6	uA
Average Current consumption 2	IDD2	SCL=SDA = 'H', FOUT=32.768kHz (FOUT pin CL=15pF), /IRQ=OFF,VDD=VIO=3.0V, CHGEN=0b or VBAT≧VDET3,-40℃~85℃		2.0	7.8	uA
Average Current consumption 3	IDD3	SCL, SDA = 'L', VBAT=3.0V, VDD=VIO=0V, -40℃~+85℃		0.9	5.0	uA
Detector Threshold voltage1 （VDD rising edge）	+VDET11	/RST releases setting:2.75 V	2.71	2.80	2.89	V
Detector Threshold voltage1 （VDD falling edge）	-VDET11	/RST output setting:2.75 V	2.66	2.75	2.84	V
Detector Threshold voltage2 （VDD rising edge）	+VDET12	/RST releases setting:2.80V	2.76	2.85	2.94	V
Detector Threshold voltage2 （VDD falling edge）	-VDET12	/RST output setting:2.80 V	2.71	2.80	2.89	V
Detector Threshold voltage3 （VDD rising edge）	+VDET2	Exchange voltage：VBAT to VDD	1.49	1.59	1.69	V



Parameter	Symbol	Condition		Value			Unit
				Min.	Typ.	Max.	
Detector Threshold voltage3 (V_{DD} falling edge)	-VDET2	Exchange voltage: VDD to VBAT		1.46	1.56	1.56	V
Detector Threshold voltage4 (V_{BAT} rising edge)	+VDET31	Stop charging voltage (full charge) BFVSEL=00b		2.94	3.02	3.10	V
Detector Threshold voltage4 (V_{BAT} falling edge)	-VDET31	Recharge voltage. BFVSEL=00b		2.89	2.97	3.05	V
Detector Threshold voltage5 (V_{BAT} rising edge)	+VDET30	Stop charging voltage (full charge) BFVSEL=10b		2.84	2.92	3.00	V
Detector Threshold voltage5 (V_{BAT} falling edge)	-VDET30	Recharge voltage. BFVSEL=10b		2.79	2.87	2.95	V
Detector Threshold voltage6 (V_{BAT} rising edge)	+VDET32	Stop charging voltage (full charge) BFVSEL=01b		3.00	3.08	3.16	V
Detector Threshold voltage6 (V_{BAT} falling edge)	-VDET32	Recharge voltage. BFVSEL=01b		2.95	3.03	3.11	V
V_{BAT} off voltage	-VDET4	Low V_{BAT} detection VBLF = 1b		2.32	2.40	2.48	V
V_{DD}-V_{OUT} Off-leak current	I_{SW1}	V_{DD}=0V, V_{OUT}=3.0V				5	nA
V_{DD}-V_{OUT} Off-leak current	I_{SW2}	V_{OUT}=0V, V_{BAT}=3.0V				5	nA
V_{OUT} output voltage1	V_{OUT1}	V_{DD}=3V, I_{OUT}=1mA			V_{DD}-0.06V		V
V_{OUT} output voltage2	V_{OUT2}	V_{BAT}=3.0V, I_{OUT}=0.1mA			V_{BAT}-0.02V		V
Input voltage High-level	V_{IH}	SCL, SDA		0.8xV_{IO}		5.5	V
Input voltage Low-level	V_{IL}			GND-0.3		0.2xV_{IO}	V
Output voltage High-level	V_{OH}	I_{OH} = -1mA	FOUT	V_{IO}-0.5		VIO	V
Output voltage Low-level	V_{OL1}	I_{OL} = 1mA	FOUT	GND		GND+0.5	V
	V_{OL2}	V_{IO}=5.0V, I_{OL}=1mA	/RST, /INT	GND		GND+0.25	V
	V_{OL3}	V_{IO}=3.0V, I_{OL}=1mA		GND		GND+0.4	V
	V_{OL4}	V_{IO}≥2.0V, I_{OL}=3mA	SDA	GND		GND+0.4	V



1.5 AC Characteristics

Table 5. AC Characteristics

Unless otherwise specified, GND =0V, V_{IO} =1.6V ~ 5.5V; Ta=-40℃ ~ +85℃

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
SCL clock frequency	fSCL				400	kHz
SCL low level time	tLOW		1.3			us
SCL high level time	tHIGH		0.6			us
Start condition setup time	tHD;STA		0.6			us
Start condition hold time	tSU;STA		0.6			us
Stop condition setup time	tSU;STO		0.6			us
Bus idle time between start condition and stop condition	tRCV		1.3			us
Data setup time	tSU;DAT		100			ns
Data hold time	tHD;DAT		0			ns
SCL, SDA rising time	tr				0.4	us
SCL, SDA falling time	tf				0.4	us

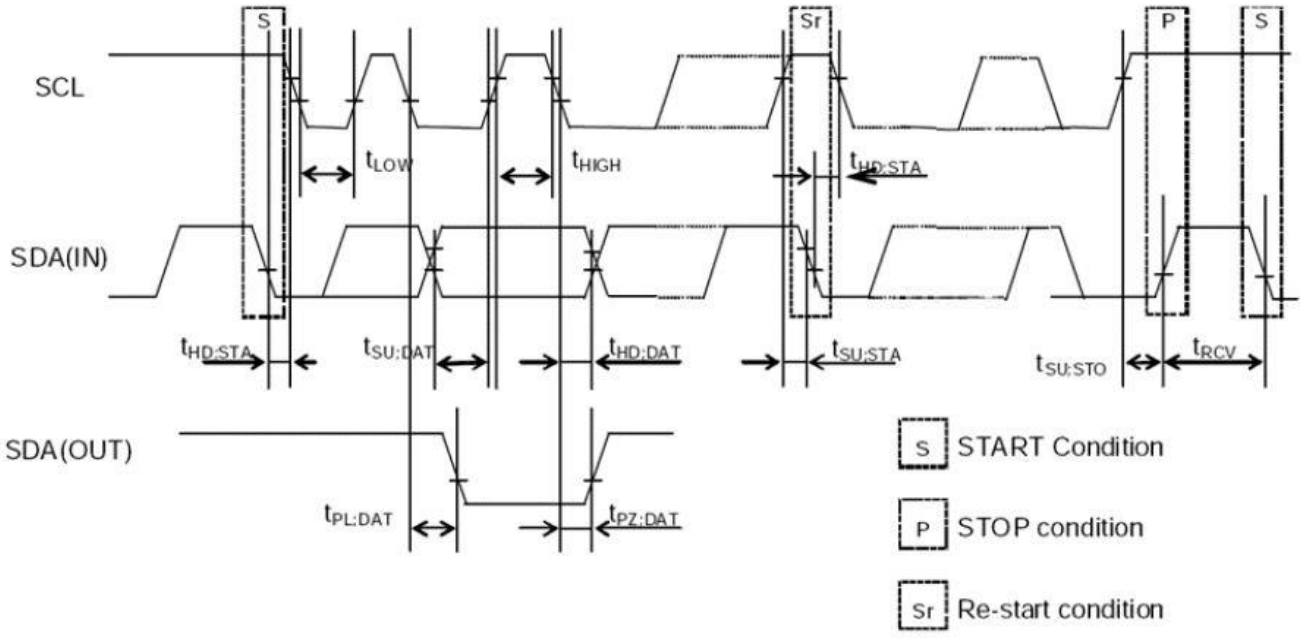
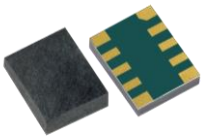


Figure 1. I^2C bus Timing Chart



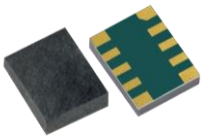
REGISTERS

2.1 Register Lists

Address 0x10~0x19: Basic Time and Calendar Registers
Address 0x1A~0x1F: Control, Flags、Extended Register sets
Address 0x20~0x23: RAM Register Bank
Address 0x30~0x31: Extended Register Bank 1

Table 6. Basic Time and Calendar Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x10	SEC	o	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				R/W
0x11	MIN	o	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				R/W
0x12	HOUR	o	o	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				R/W
0x13	WEEK	o	6	5	4	3	2	1	0	R/W
0x14	DAY	o	o	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				R/W
0x15	MONTH	o	o	o	BCD code, Month tens place, 0-3	BCD code, Day ones place, 0-9				R/W
0x16	YEAR	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9				R/W
0x17	MIN Alarm	AE	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				R
0x18	HOUR Alarm	AE	•	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				R/W
0x19	WEEK Alarm	AE	6	5	4	3	2	1	0	R/W
	DAY Alarm		•	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				R/W
0x1A	Timer Counter 0	128	64	32	16	8	4	2	1	R/W
0x1B	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256	R/W
0x1C	Extension Register	FSEL[1]	FSEL[0]	USEL	TE	WADA	TSEL[2]	TSEL[1]	TSEL[0]	R/W
0x1D	Flag Register	VBLF	o	UF	TF	AF	RSF	VLF	VBFF	R/W
0x1E	Control Register	TEST	STOP	UIE	TIE	AIE	TSTP	TBKON	TBKE	R/W
0x1F	Control Register	SMP TSEL[1]	SMP TSEL[0]	CHGEN	INIEN	○	RSVSEL	BF VSEL[1]	BF VSEL[0]	R/W
0x20 – 0x23	RAM	•	•	•	•	•	•	•	•	R/W
0x30	Digital offset	DTE	L7	L6	L5	L4	L3	L2	L1	R/W
0x31	Extension Register1	○	○	○	○	○	○	○	VBLFE	R/W



Note:

1. After power-up reset or in case VLF bit returns “1”, make sure to initialize all registers to default state before using the RTC. 2.

2. During the initial power-up, below bits will be in the state as below:

   Initial 0: TEST、WADA、USEL、TE、FSEL[1:0]、TSEL[2:0]、UF、TF、AF、UIE、TIE、AIE、TSTP、TBKON、TBKE、DTE、 VBLF、VBFF、SMPTSEL[1:0]、CHGEN、INIEN、RSVSEL、BFVSEL[1:0]、VBLFE；

   Initial 1: VLF、RSF；

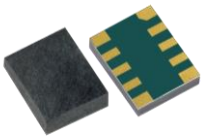
3. All other register values are undefined, so make sure to reset the module before using it.

4. The bits marked with “o” can be read out “0” only after initializing.

5. The bits marked with “●” are RAM bits which can be used to write or read any data.

6. Only 0 can be written to UF, TF, AF, VLF bits.

7. Make sure “0” to be written for TEST bits which are used for testing only



2.2 Details of Registers

2.2.1 Clock Counter Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x00/10	SEC	O	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				0x00
0x01/11	MIN	O	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				0x00
0x02/12	HOUR	O	O	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				0x00

SEC: BCD format, Value: 0~59

MIN: BCD format, Value: 0~59

HOUR: BCD format, Value: 0~23

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x13	WEEK	O	6	5	4	3	2	1	0	0x40

WEEK: Value 01h, 02h, 04h, 08h, 10h, 20h, 40h. Only one bit can be set to 1 each time, all others must be set to 0.

Table 7. WEEK Register

WEEK	Data	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sunday	01h	0	0	0	0	0	0	0	1
Monday	02h	0	0	0	0	0	0	1	0
Tuesday	04h	0	0	0	0	0	1	0	0
Wednesday	08h	0	0	0	0	1	0	0	0
Thursday	10h	0	0	0	1	0	0	0	0
Friday	20h	0	0	1	0	0	0	0	0
Saturday	40h	0	1	0	0	0	0	0	0

Only one bit can be set to one at a time.

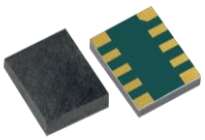
Table 8. Daily Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x14	DAY	O	O	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				0x01

DAY: BCD format, the value range will be adjusted automatically according to the month setting and if a leap year or not .

Table 9. DAY Register Value

Month	Day Value Range
1, 3, 5, 7, 8, 10, 12	1~31
4, 6, 9, 11	1~30
February in normal year	1~28
February in leap year	1~29



Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x15	MONTH	O	O	O	BCD code, Month tens place, 0-1	BCD code, Month ones place, 0-9				0x01
0x16	YEAR	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9				0x00

MONTH: BCD format, Value 1~12

YEAR: BCD format, Value 0~99(2000~2099)

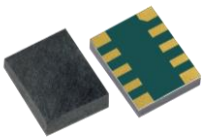
Example: 2020/01/01 Wednesday 21:18:36

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x10	SEC	O	0	1	1	0	1	1	0
0x11	MIN	O	0	0	1	1	0	0	0
0x12	HOUR	O	O	1	0	0	0	0	1
0x13	WEEK	O	0	0	0	1	0	0	0
0x14	DAY	O	O	0	0	0	0	0	1
0x15	MONTH	O	O	O	0	0	0	0	1
0x16	YEAR	0	0	1	0	0	0	0	0

2.2.2 Alarm Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x17	MIN Alarm	AE	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				0x00
0x18	HOUR Alarm	AE	●	BCD code, Hour tens place, 0-2		BCD code, Minute ones place, 0-9				0x00
0x19	WEEK Alarm	AE	6	5	4	3	2	1	0	0x00
	DAY Alarm		●	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				

1. Set specific day, week, hour, minute value, cooperate with AIE, AF, WADA, generate alarm interrupt;
2. WEEK Alarm/DAY Alarm: WADA bit control 0x0A is set for daily or weekly Alarm. For details, see 0x1C register bit3;
3. AE (Alarm Enable): Alarm Alarm control, 0- Enable. 1 - to enable;
4. AF function bit see 0x1D register bit3;
5. AIE function bit see register 0x1E bit3 for details;



2.2.3 Timer Control Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x1A	Timer Counter 0	128	64	32	16	8	4	2	1	0x00
0x1B	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256	0x00

According to TE, TF, TIE, TSEL[1:0] bits setting, a timer interrupt will be generated once the value counts down to 0 from the one set in the above registers.

TE: Defined in 0x0D register bit4

TF: Defined in 0x0E register bit4

TIE: Defined in 0x0F register bit4

TSEL[1:0]: Defined in 0x0D register bit1 and bit0

2.2.4 Extension Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x1C	Extension Register	FSEL [1]	FSEL [0]	USEL	TE	WADA	TSEL [2]	TSEL [1]	TSEL [0]	0x00

1. Alarm function, time update interrupt, Settings, etc. used to specify a specific target;
2. WADA (Week Alarm/Day Alarm) : 0-WEEK Alarm, 1-DAY Alarm;
3. USEL (Update Interrupt Select) : 0-interrupts per second (default), 1-interrupts per minute;
4. TE (Timer Enable) : 0- Disables the Timer interrupt function. 1- enables the Timer interrupt function

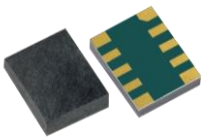
FSEL[1], FSEL[0]: FOUT frequency setting:

FSEL[1]	FSEL[0]	FOUT Frequency
0	0	32.768kHz (Default)
0	1	1024Hz
1	0	1Hz
1	1	off

When STOP is to set to 1, the output is 32768Hz and 1024Hz, but not 1Hz

TSEL[2], TSEL[1], TSEL[0]: timer count clock selection, as shown in the following table:

TSEL[2]	TSEL[1]	TSEL[0]	Source clock	
0	0	0	4096Hz（244.14us）	122uS
0	0	1	64Hz（15.625ms）	7.57mS
0	1	0	1Hz（1 second）	7.57mS
0	1	1	1/60Hz（1 minute）	7.57mS
1	0	0	1/3600Hz（1 hour）	7.57mS



2.2.5 Flag Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x1D	Flag Register	VBLF	○	UF	TF	AF	RSF	VLF	VBFF	0x06

UF（Update Flag）：Time update flag bit that changes from "0" to "1" when a time update interrupt event occurs and remains "1" until software writes "0";

TF（Timer Flag）：Timer flag bit that changes from "0" to "1" when a fixed periodic interrupt occurs and remains "1" until software writes "0".

AF（Alarm Flag）：Alarm flag bit that changes from "0" to "1" when an alarm interrupt occurs and remains "1" until the software writes "0".

VLF（Voltage Low Flag）：Voltage low signal, when the voltage is lower than 1.59V, set "1" and keep "1" until software write "0".

VBFF（VBAT Full Charged Flag）：Rechargeable battery charging flag. "0" means charging, "1" means charging completed, updated every second.

VBLF（VBAT Low Flag）：Battery low voltage indicator. Set"1" when voltage is lower than VDET4 and keep "1" until software writes "0";

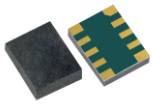
RSF（Reset Flag）：Reset flag. Set '1' when voltage is below -vdet1 and keep"1"until software writes "0"' ;

Table10. RSF Settings

RSF	Description	Note
0	Clear 0	Write operation
1	Disallow operations (write 1 is ignored)	
0	-	Read operation
1	V_{BAT} lower than -V_{DET} detected	

Table11. VBLF Settings

VBLF	Describe	Note
0	Clear 0	Write operation
1	Disallow operations (write 1 is ignored)	
0	-	Read operation
1	Voltage below V_{DET4} detected	



2.2.6 Control Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x1E	Control Register 0	TEST	STOP	UIE	TIE	AIE	TSTP	TBKON	TBKE	0x00
0x1F	Control Register 1	SMPTSEL [1]	SMPTSEL [0]	CHGEN	INIEN	o	RSVSEL	BFVSEL[1]	BFVSEL [0]	0x00

TEST ： The manufacturer test bit must be 0 and cannot be modified by users;
UIE: Update Interrupt Enable bit. When UF changes from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disenable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).
TIE: Timer Interrupt Enable bit: When TF changes from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disenable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).
AIE: Alarm Interrupt Enable bit: When AF changes from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disenable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low);
TSTP (Timer Stop): This bit is used to Stop the countdown of a Timer with a fixed period. It is usually used with STOP, TE, and TBKE bits;
CHGEN (Charge Enable): Charge control switch of the standby battery. CHGEN Is used for non-rechargeable batteries. The default value is 0. CHGEN position "1" for rechargeable batteries, INIEN needs both "1",
INIEN: indicates the power switch setting bit. The recommended value for initialization is 1;

Table12. INIEN Settings

INIEN	Describe	Note
0	1. I2C and FOUT functions are available ； 2. Power switching function is available ； 3. The CHGEN bit function is disabled. That's the same thing as CHGEN=0 ； 4. Be careful not to input intermediate voltage to the I2C interface ；	When writing “0”, you are advised to write “1” before “0”;
1	1. When VDD < VDET1, I2C and FOUT functions are unavailable ； 2. When VDD is greater than VDET1, I2C and FOUT functions are available ； 3. CHGEN is available ；	

STOP: used to STOP the timing operation. When "STOP=1", all timing updates and calendar operations STOP; Fixed period timer interrupt function partially stops; 32768Hz and 1024Hz can be output, but 1Hz output is disabled;

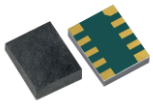


Table13. Fixed-period timer stop control (TSTP setting)

TE	STOP	TBKE	TSTP	Note
1	0	0	0	TSTP writing "0" will restart the timer countdown.
			1	TSTP writes "1" to stop the timer
		1	x	The TSTP value setting is invalid and the count does not stop even if set in TSTP= "1".
	1	x	x	The timer stops when it is set to 64Hz, 1Hz, 1/60Hz or 1/3600Hz.
0	x	x	x	no counting

TBKON (Timer Backup On)、TBKE (Timer Backup Enable)： which is used to select the working time of the main power supply or the backup power supply. The count value is added.

Table14. Fixed-period timer normal mode/backup mode control

TBKE	TBKON	Note
1	0	This setting counts it at time of VDD supply mode
	1	This setting counts it at time of VBAT supply mode
0	x	This setting counts on VDD supply mode and VBAT supply mode

SMPTSEL [1:0] (Sampling Time Select), for determining voltage detection period.

Table15. VDET3, VDET4 intermittent detection period

SMPTSEL [1:0]	VDD work (Battery charging)	VDD work (Battery charging completed)	VDD work (Return from backup mode, VDET1>VDD>VDET2)	Note
00	2ms	2ms	2ms	The default 00
01	16ms	16ms	2ms	
10	128ms	128ms	2ms	
11	256ms	256ms	2ms	

RSVSEL (Reset Voltage Select): Sets VDD pin Voltage detection level. VDET1 voltage level setting. If VDD drops below this level, output /RST signal and stop I/F and FOUT output (depending on INIEN bit Settings)

Table16. RSVSEL Settings

RSVSEL	Describe	Note
0	2.75V	- V_{DET11}
1	2.80V	-V_{DET12}

BFVSEL [1:0]: Setting the full charge detection threshold voltage to stop charging of the backup battery.

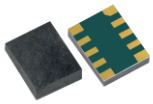


Table18. BFVSEL Settings

BFVSEL [1]	BFVSEL [0]	Describe
0	0	3.02V
0	1	3.08V
1	0	2.92V
1	1	Off (unlimited charging)

2.2.7 Digital offset register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x30	Digital offset	DTE	L7	L6	L5	L4	L3	L2	L1	0x00

DTE (Digital offset function Enable): Enables the digital offset adjustment function. If DET is “1”, digital offset adjustment is enabled. DET is “0” to turn off digital offset adjustment; After the digital offset function is enabled, the digital offset register adjusts the sub-second clock according to the value set in the digital offset register. The calibration of the "seconds" register takes place every 10 seconds and the amount of offset set determines the intensity of the calibration. This feature does not affect the 32.768 kHz signal output on the FOUT pin because it does not change the oscillation frequency of the built-in crystal. In the case of 1Hz or 1024Hz signal output on FOUT, the offset correction will cause some jitter on the clock signal. The alarm function and wake timer function (if a source clock less than 4096 Hz is selected) are affected by this function The following table shows the corresponding offset value from L7 to L1. When L7 bit is “0”, the offset value is positive (the clock runs faster) and when L7 bit is “1” the offset value is negative (the clock runs slower) :

Table19. Digital offset registers

L7	L6	L5	L4	L3	L2	L1	Offset Value (ppm)
0	1	1	1	1	1	1	+192.26
0	1	1	1	1	1	0	+189.21
…	……						…
0	0	0	0	0	1	0	+6.1
0	0	0	0	0	0	1	+3.05
0	0	0	0	0	0	0	±0
1	1	1	1	1	1	1	-3.05
1	1	1	1	1	1	0	-6.1
…	……						…
1	0	0	0	0	0	1	-192.26
1	0	0	0	0	0	0	-195.31

Digital offset calculation method is as follows.

When the offset value is positive, L [7:1] = [Offset Value]/3.05, decimals are discarded.

When the offset value is negative, L [7:1] = 128- [Offset Value]/3.05, decimals are discarded.

2.2.8 Battery Backup Switchover Register

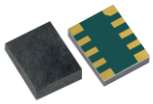
Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x31	Extension Register 1	O	O	O	O	O	O	O	VBLFE	0x00

VBLFE (VBAT Low Flag Enable) : enables the battery Low voltage detection function；

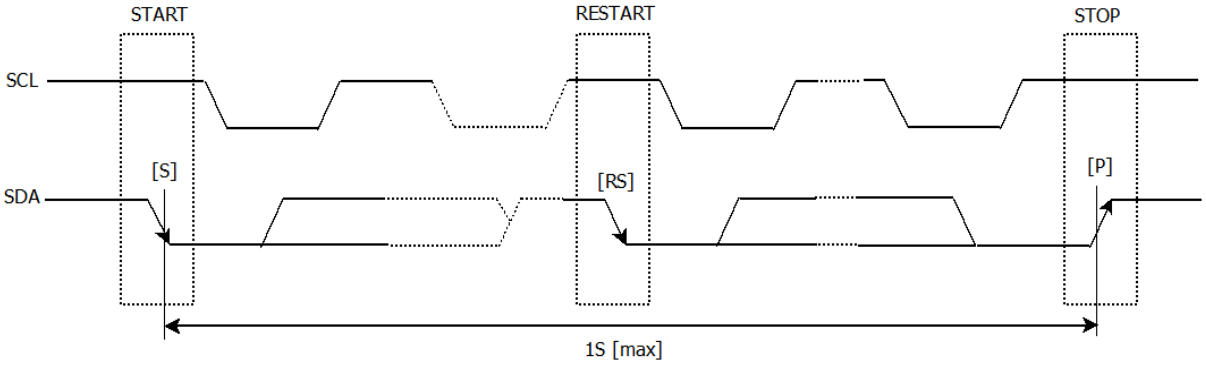
Table19. VBLFE Settings

Operation	VBLFE	Describe
Write	0	CHGEN:0 VBLF detection not enable CHGEN:1 VBLF detection enable (during normal mode re-chargeable battery charging)
	1	VBLF detection enable during VDD supply

If you want to use VBLF detection, the INIEN should be set to 1 in addition to VBLFE bit setting. In VDD drive mode VBAT low voltage (non-rechargeable, rechargeable battery) can be detected. VBLF function is not available in case of backup mode.



I²C Bus Interface



I²C bus supports bi-directional communications through a serial clock line SCL and a serial data line SDA. I²C bus device can be defined as “Master” and “Slave”. RTT21064 can only be used as Slave.

3.1 Cautions

I2C bus includes START, RESTART, STOP conditions, the duration between START and STOP must be less than 1 second just in case the bus to be set to standby mode automatically. A new START condition must be transferred before restarting of any communications

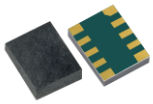
RTT21064 I²C bus interface supports single byte read/write operations as well as multiple bytes incremental access. After 0x7F address, the next one will be 0x00.

3.2 Slave Address

Table 20. I²C Bus Slave Address

Transfer data	Slave address							R/W
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
65h (Read)	0	1	1	0	0	1	0	1 (Read)
64h (Write)								0 (Write)

RTT21064 I²C bus Slave Address is [0110 010*].



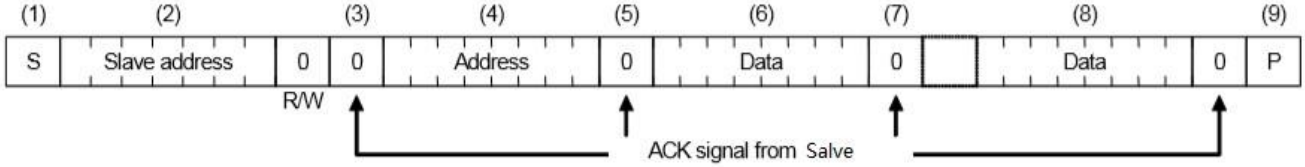
3.3 I²C bus Protocol

It is assumed CPU is master and **RTT21064** is slave in this section.

3.3.1 Write Process

I²C bus includes an address auto-increment function, once the initial address has been specified, the **RTT21064** increments (+1) the address automatically after each data is sent, then to write next data.

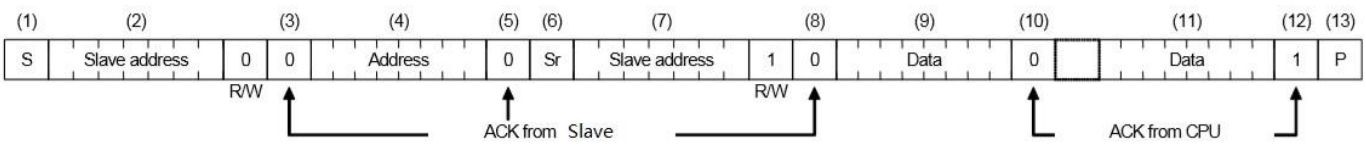
(1) CPU sends start condition[S]
(2) CPU sends **RTT21064**'s slave address with R/W bit to set to write mode
(3) CPU verifies ACK signal from **RTT21064**
(4) CPU sends write address to **RTT21064**
(5) CPU verifies ACK signal from **RTT21064**
(6) CPU sends write data to the address specified at step (4)
(7) CPU verifies ACK signal from **RTT21064**
(8) Repeat (6) (7) if multiple bytes need to be written, address will be incremented automatically
(9) CPU ends stop condition[P]

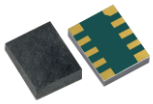


3.3.2 Read Process

Writing the address to be read with write mode firstly, then reading the data with read mode.

(1) CPU sends start condition[S]
(2) CPU sends **RTT21064**'s slave address with R/W bit to set to write mode
(3) CPU verifies ACK signal from **RTT21064**
(4) CPU sends address for reading from **RTT21064**
(5) CPU verifies ACK signal from **RTT21064**
(6) CPU sends RESTART condition [Sr]
(7) CPU sends **RTT21064**'s slave address with R/W bit to set to read mode
(8) CPU verifies ACK signal from **RTT21064**
(9) CPU reads data from the specified address in step (4)
(10) CPU verifies ACK signal from **RTT21064**
(11) Repeat (9) (10) if multiple bytes need to be read, address will be incremented automatically
(12) CPU sends ACK signal for "1"
(13) CPU sends stop condition[P]





MECHANICAL CHARACTERISTICS

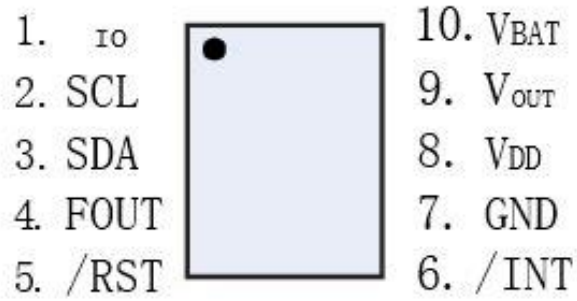


Table21. Pin Function

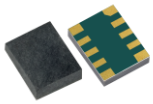
Pin Number	Pin Name	I/O	Description
1	V_{IO}	-	Interface power supply pin.
2	SCL	In	I^2C clock signal
3	SDA	In/Out	I^2C data signal
4	FOUT	Out	Frequency output. Frequency can be set by FSEL bits.
5	/RST	Out	Reset signal output. After the VDD pressure drop is detected, the pin outputs a negative pulse.
6	/INT	Out	Timing event interrupt output. Open-Drain.
7	GND	-	Ground
8	V_{DD}	-	Power supply
9	V_{OUT}	-	Internal voltage output pin. Connect capacitor of 1.0uF to Ground
10	V_{BAT}	-	Backup battery pin. Connect to large-capacity capacitors or a backup battery. Connect to V_{DD} when switchover function is not necessary

Note: A 0.1µF bypass capacitor is needed at least between power supply pins and GND pin.

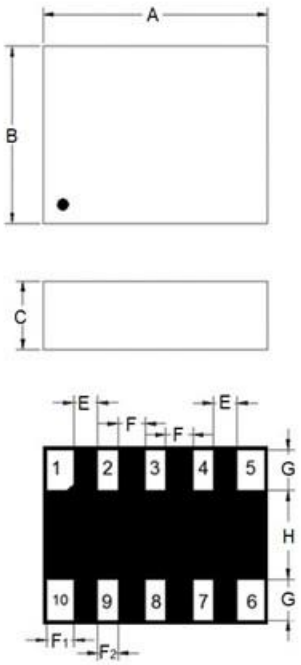
Note: Input pins regardless of VIO applied voltage. It is able to input up to 5.5V.

Note: Open drain pins regardless of VIO applied voltage. It is able to Pull-up to 5.5V

Note: When not use, take the FOUT, /RST, /IRQ terminals as OPEN

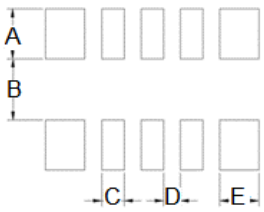


DIMENSIONS



Dimension	Min.	Typ.	Max.
A	3.0	3.2	3.4
B	2.3	2.5	2.7
C	--	1.0	--
E	--	0.3	--
F	--	0.4	--
G	--	0.6	--
H	--	1.3	--
F1	--	0.45	--
F2	--	0.3	--

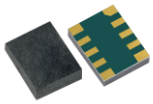
Figure 2. Dimension



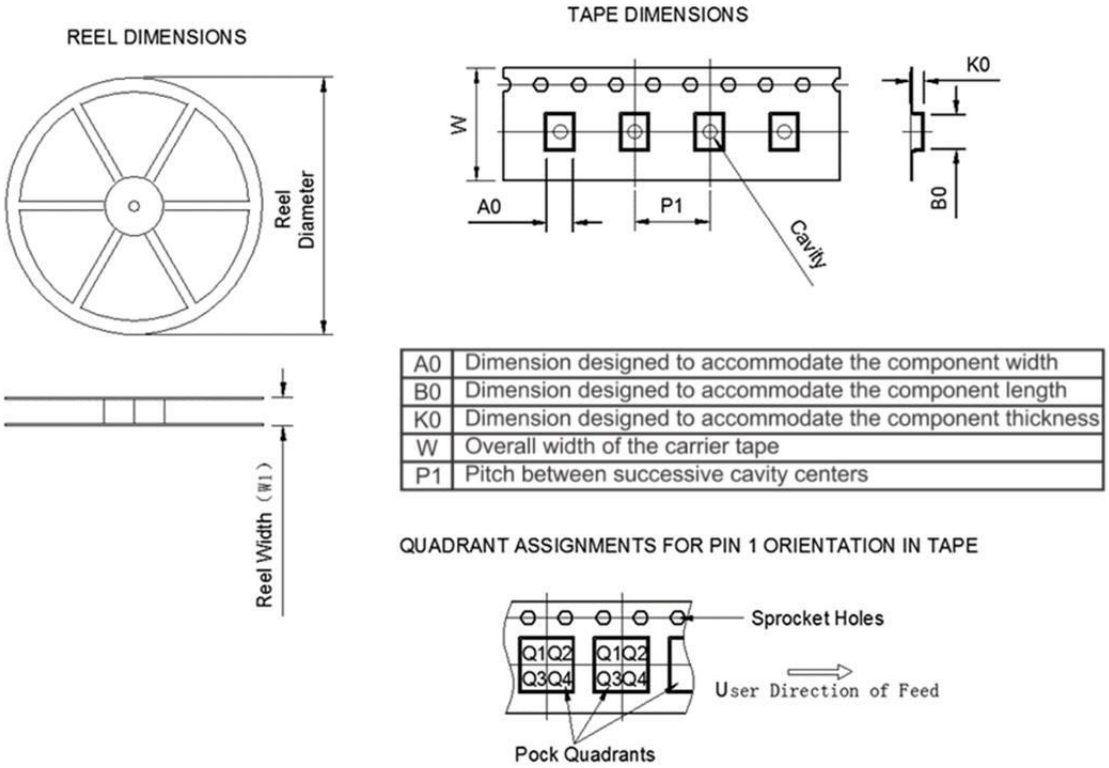
Dimension	Max.
A	0.9
B	1.1
C	0.4
D	0.3
E	0.7

(Unit: mm)

Figure 3. Recommended Soldering Pattern



PACKAGE



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Pins	Reel Diameter (mm)	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
10	180	11.6±2.0	3.00	3.70	1.50	4.00	8.00

Figure 4. Package

- **APPROVAL**

DRAWN BY:	AR, October 08, 2021
APPROVED BY:	CP, October 08, 2021
REVISION:	A, Initial Release
	B, AR, December 13, 2021 Updated the Current Revision Levels
	C, AR, May 23, 2022 Updated the Current Revision Levels