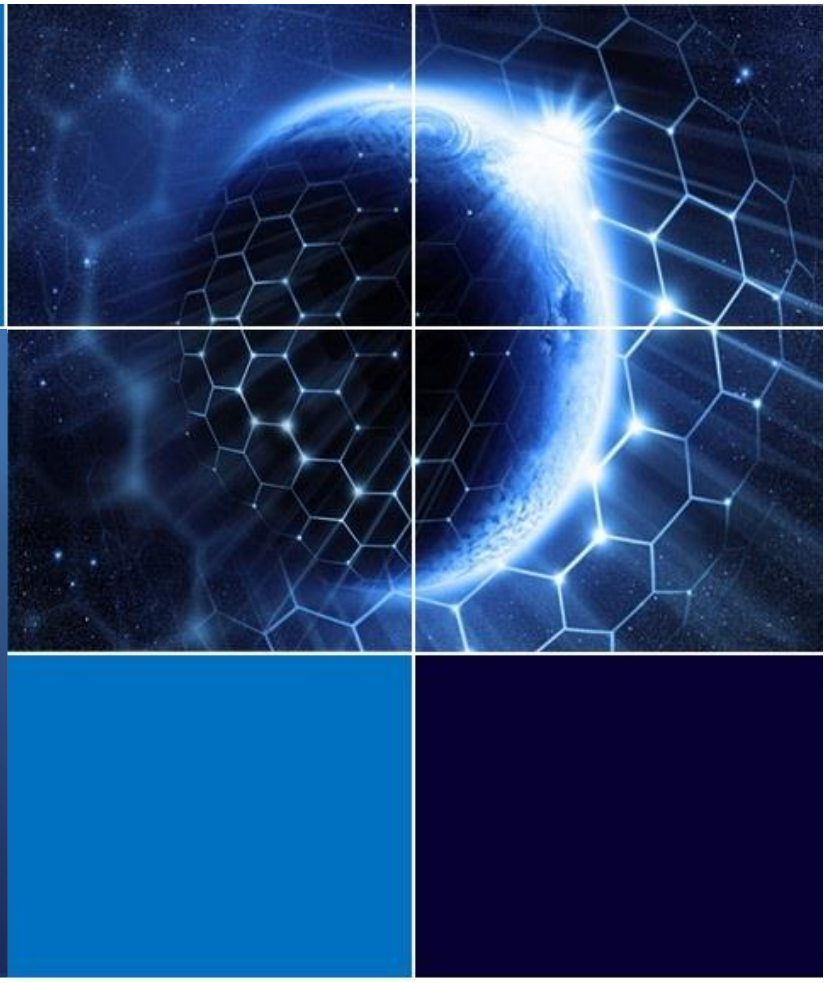
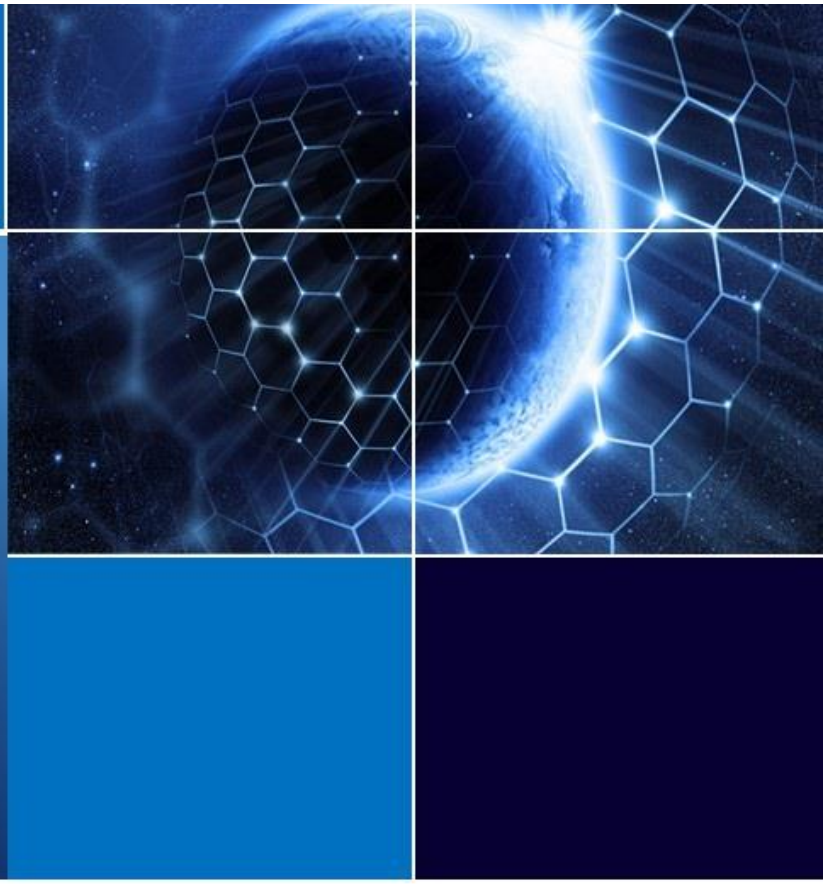


Ultra-low Jitter High Frequency LVDS Clock Oscillators

User's Guide



Application Note OSCLVDS-July 2020

RALTRON ELECTRONICS ▪ 10400 N.W. 33rd Street ▪ Miami, Florida 33172 ▪ U.S.A.
Telephone: +1-305-593-6033 ▪ Fax: +1-305-594-3973 ▪ e-mail: sales@raltron.com ▪ internet: http://www.raltron.com

LVDS Oscillators
Recommendations for Circuit Configuration, Test Set-Up and Power-Supply Noise Rejection Optimization

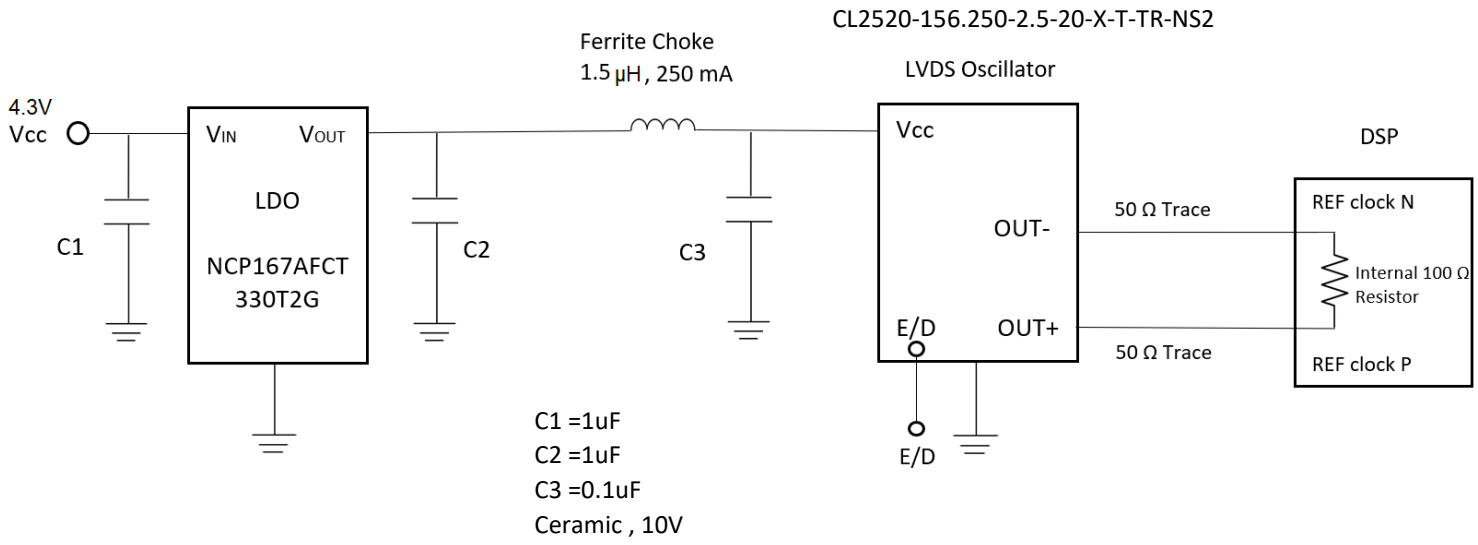
Table of Contents

This Application Note is offering recommendations for:

RALTRON ELECTRONICS ▪ 10400 N.W. 33rd Street ▪ Miami, Florida 33172 ▪ U.S.A.
Telephone: +1-305-593-6033 ▪ Fax: +1-305-594-3973 ▪ e-mail: sales@raltron.com ▪ internet: http://www.raltron.com

Circuit Configuration and PCB Layout Recommendations

Circuit Configuration 0
Complete Circuit

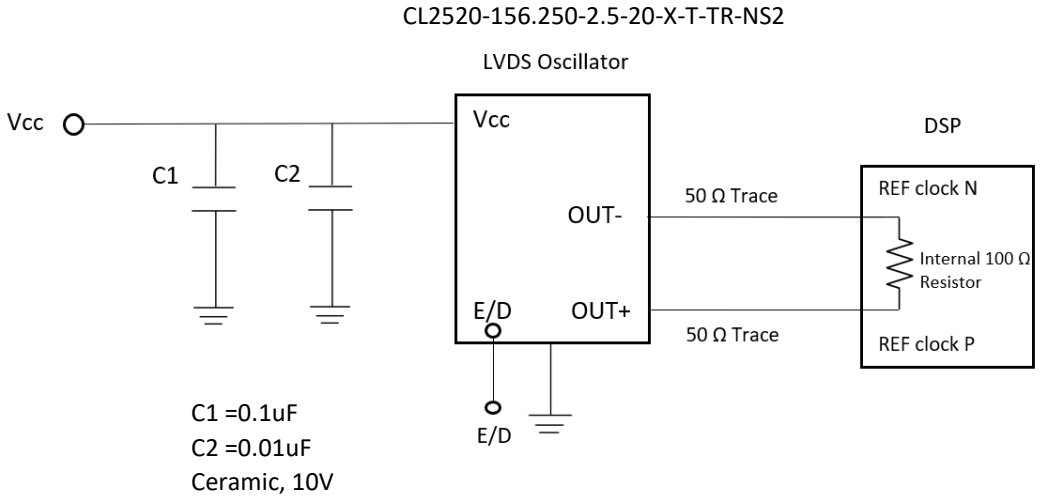


Complete Circuit Configuration using LDO, choke and capacitors.
Offers excellent Power Supply Noise Reduction but uses excessive space and is costly because of the large number of components used. Recommended only for applications where space is not at a premium.

RALTRON ELECTRONICS ▪ 10400 N.W. 33rd Street ▪ Miami, Florida 33172 ▪ U.S.A.
Telephone: +1-305-593-6033 ▪ Fax: +1-305-594-3973 ▪ e-mail: sales@raltron.com ▪ internet: http://www.raltron.com

Circuit Configuration and PCB Layout Recommendations

Circuit Configuration 1
By-Pass Capacitors Only

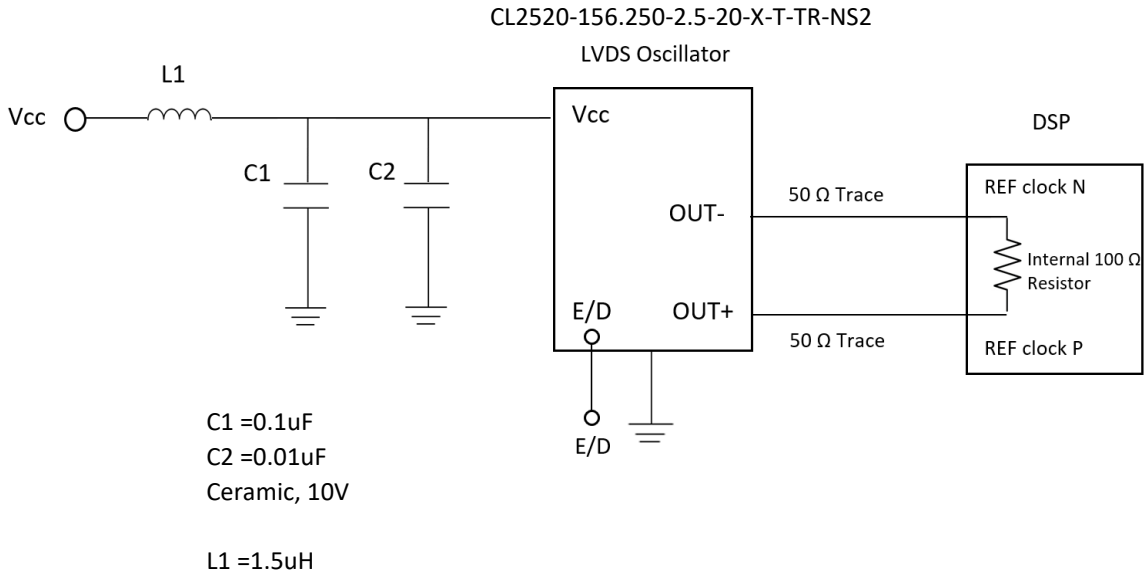


Simple Circuit Configuration using only filtering capacitors.
Offers reasonable Power Supply Noise Reduction based mostly on the Oscillator internal filtering but uses optimum space and is not costly because of the limited number of components used. Recommended only for applications where the on-board power supply is reasonably clean.

RALTRON ELECTRONICS ▪ 10400 N.W. 33rd Street ▪ Miami, Florida 33172 ▪ U.S.A.
Telephone: +1-305-593-6033 ▪ Fax: +1-305-594-3973 ▪ e-mail: sales@raltron.com ▪ internet: http://www.raltron.com

Circuit Configuration and PCB Layout Recommendations

Circuit Configuration 2
Ferrite Choke and By-Pass Capacitors

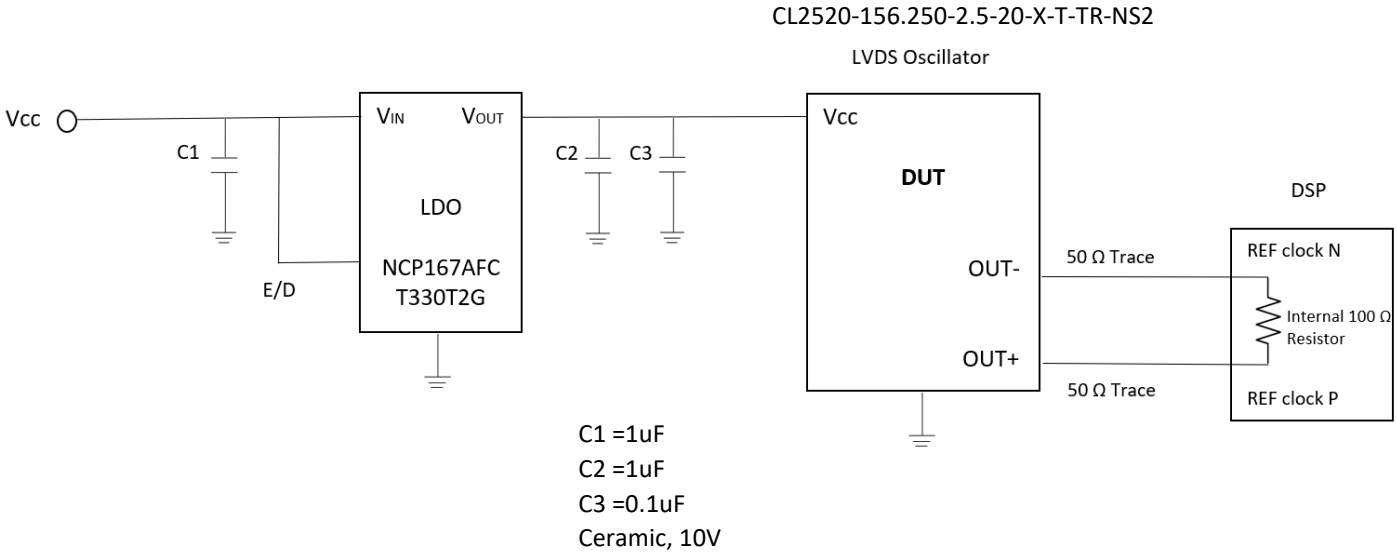


Simple Circuit Configuration using filtering capacitors and choke.
Offers better Power Supply Noise Reduction than Circuit Configuration 1 because of the additional noise suppression by the choke. Uses increased space and is more costly because of the additional component used. Recommended only for applications where the on-board power supply has an average noise level and space is not at a premium.

RALTRON ELECTRONICS ▪ 10400 N.W. 33rd Street ▪ Miami, Florida 33172 ▪ U.S.A.
Telephone: +1-305-593-6033 ▪ Fax: +1-305-594-3973 ▪ e-mail: sales@raltron.com ▪ internet: http://www.raltron.com

Circuit Configuration and PCB Layout Recommendations

Circuit Configuration 3
LDO and By-Pass Capacitors



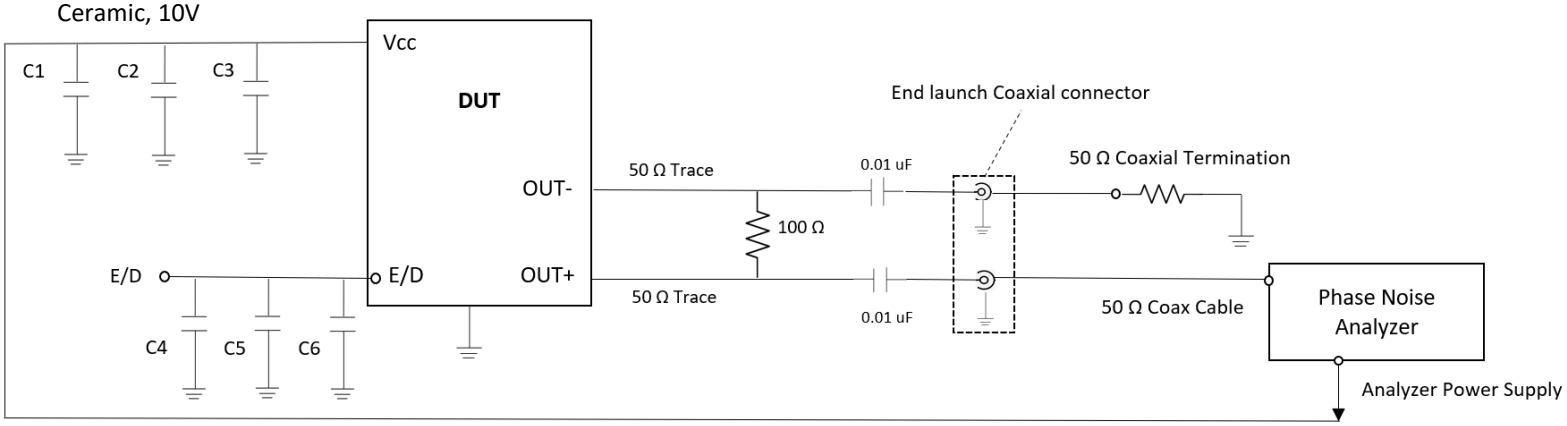
Simplified Circuit Configuration using LDO and filtering capacitors.
Offers better Power Supply Noise Reduction than Circuit Configuration 1 and 2 because of the superior noise reduction provided by the LDO. PCB space utilization is optimized because of the very small size of the LDO selected. This solution is recommended for applications such as small format optical transceivers where space is at a premium and increased PSRR is desired.

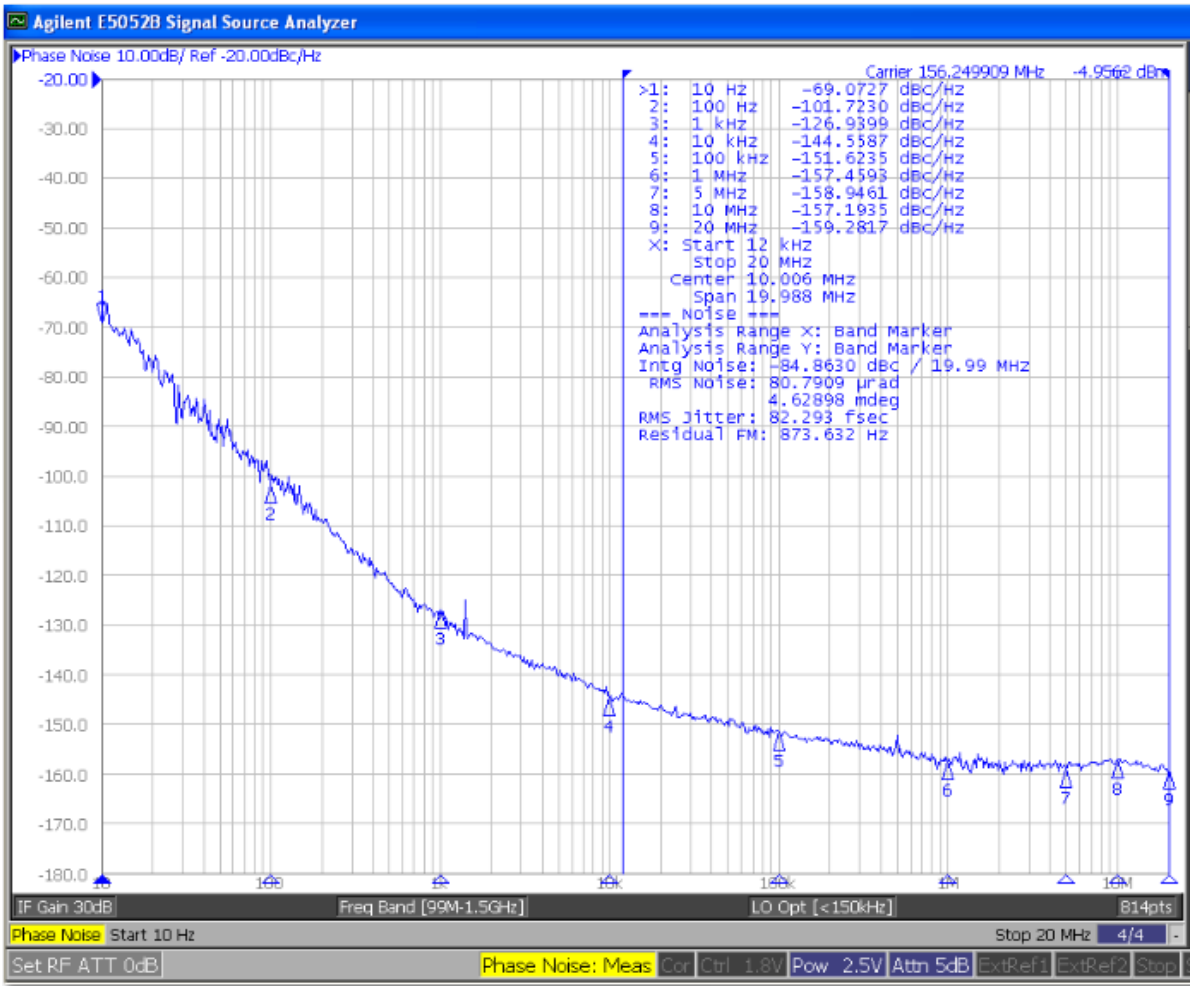
RALTRON ELECTRONICS ▪ 10400 N.W. 33rd Street ▪ Miami, Florida 33172 ▪ U.S.A.
Telephone: +1-305-593-6033 ▪ Fax: +1-305-594-3973 ▪ e-mail: sales@raltron.com ▪ internet: http://www.raltron.com

Phase Noise Test Circuit

C1=C4= 10uF
C2=C5= 1uF
C3=C6= 0.01uF
Ceramic, 10V

CL2520-156.250-2.5-20-X-T-TR-NS2
LVDS Oscillator



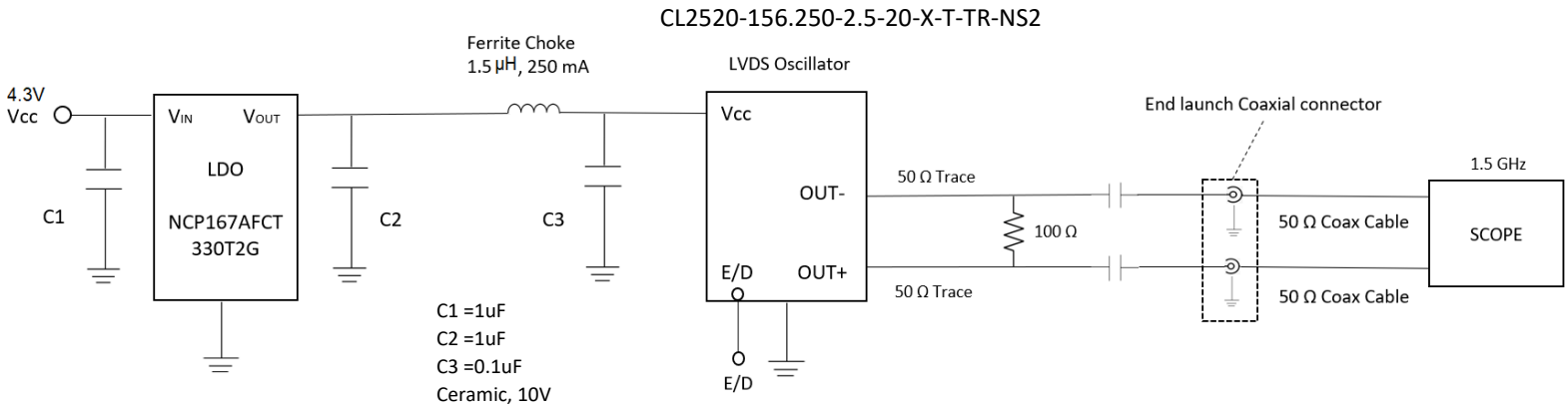


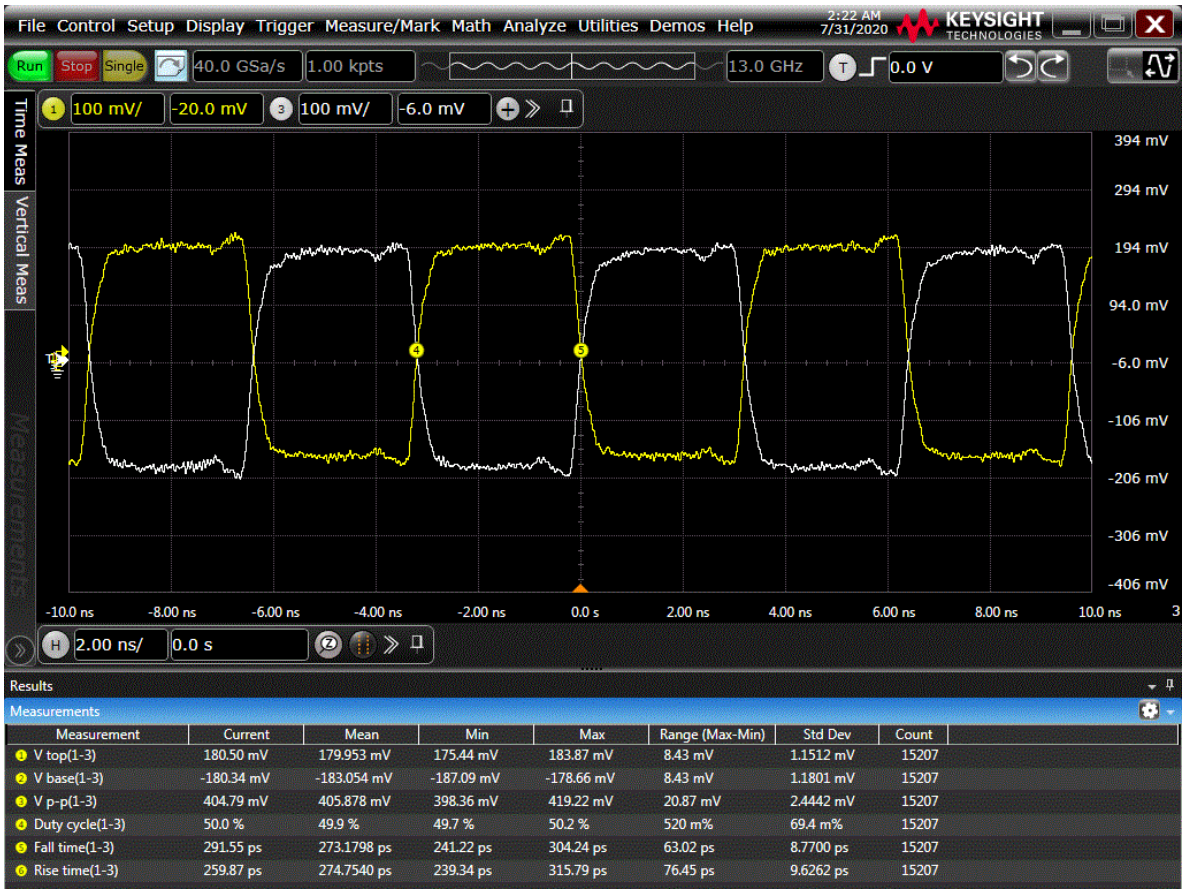
Correct oscillator phase noise plot obtained using above test circuit

RALTRON ELECTRONICS ▪ 10400 N.W. 33rd Street ▪ Miami, Florida 33172 ▪ U.S.A.
Telephone: +1-305-593-6033 ▪ Fax: +1-305-594-3973 ▪ e-mail: sales@raltron.com ▪ internet: http://www.raltron.com

Output Signal Integrity Test Circuit

- **Use clean (low ripple) linear power supply**
- **Use two 50 Ω coax cables connected with the two clock oscillator outputs.**
- **Test: Output levels, output waveform, rise & fall time, waveform symmetry**





LVDS "OUT+" and "OUT-" Waveform in Eye Diagram

(amplitudes of "OUT+" and "OUT-" around 360mV)

RALTRON ELECTRONICS ▪ 10400 N.W. 33rd Street ▪ Miami, Florida 33172 ▪ U.S.A.
Telephone: +1-305-593-6033 ▪ Fax: +1-305-594-3973 ▪ e-mail: sales@raltron.com ▪ internet: http://www.raltron.com

LVDS Oscillators Power Supply Noise Rejection Optimization

- Power supply noise rejection defines how well a circuit eliminates the effect of noise of various frequencies injected in it through its power supply input (Vcc pin). PSRR (Power Supply Rejection Ratio) is the ratio of the circuit input voltage variation to the circuit output voltage variation.

- Power supply noise rejection can be optimized by utilizing filtering circuitry. The most common filters are capacitors of various values, inductors(chokes) and linear regulators (LDOs- low drop-out regulators).

- For best results combinations of several or all these types of filters need to be used. The challenge is to find the best compromise solution between conflicting parameters: optimum PSRR which in general is proportional with the number of filtering components used, PCB space which is increasingly at premium and cost.

- The following Circuit Configurations 1-3 have been tested for PSRR performance using Raltron LVDS 156.250MHz 2520 oscillator PN CL2520-156.250-2.5-20-X-T-TR-NS2

  Datasheet: CL2520-156.250-2.5-20-X-T-TR-NS2

  The test consisted of injecting into the Oscillator Power Supply pin an AC waveform of 100 mV amplitude and measuring the Phase Noise Spurs produced at the Oscillator output for input signal frequencies of 10 kHz, 100 kHz, 1 MHz and 10 MHz. The spurs amplitudes were then compared for the three proposed circuit configurations.

RALTRON ELECTRONICS ▪ 10400 N.W. 33rd Street ▪ Miami, Florida 33172 ▪ U.S.A.
Telephone: +1-305-593-6033 ▪ Fax: +1-305-594-3973 ▪ e-mail: sales@raltron.com ▪ internet: http://www.raltron.com

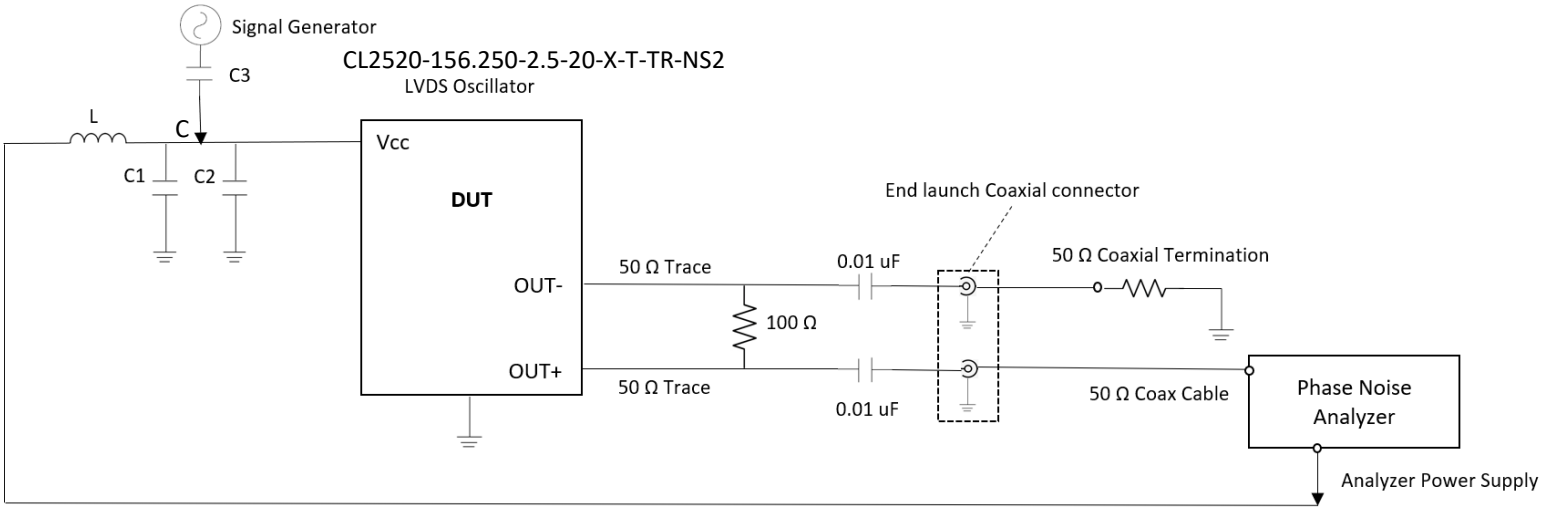
Raltron LVDS Oscillators Power Supply Noise Rejection Circuit Configurations

Circuit Configuration 1
By-Pass Capacitors Only

Test equipment: Phase Noise Analyzer Agilent E5052B, Signal Generator Agilent 33250A.
Condition: Vdd=3.3V.

An AC sinewave signal is injected into the circuit at the point C indicated below and the waveform amplitude is measured to be 100mV at the Vin pin of the LDO. The signal frequency is sequentially modified from 10kHz to 100kHz, 1MHz and 10MHz respectively and phase noise is measured in each case. The measurements are made at room temp, utilizing the circuit below,

The following components values are recommended: C1=0.1uF, C2=0.01uF, C3=20.1uF. The by-pass capacitors must be placed as close to Vcc & GND pins as possible. They are acting as low pass filters. The inductor L (L=4.7uH) is only part of the test fixture to prevent grounding of injected AC sinewave signal.



Offset Frequency from Fo	Fn =10kHz	Fn =100kHz	Fn =1 MHz	Fn =10 MHz
Phase Noise Spur Value Induced by Signal Generator [dBc/Hz]	-94.6	-120.56	-103.77	-148.18

RALTRON ELECTRONICS ▪ 10400 N.W. 33rd Street ▪ Miami, Florida 33172 ▪ U.S.A.
Telephone: +1-305-593-6033 ▪ Fax: +1-305-594-3973 ▪ e-mail: sales@raltron.com ▪ internet: http://www.raltron.com

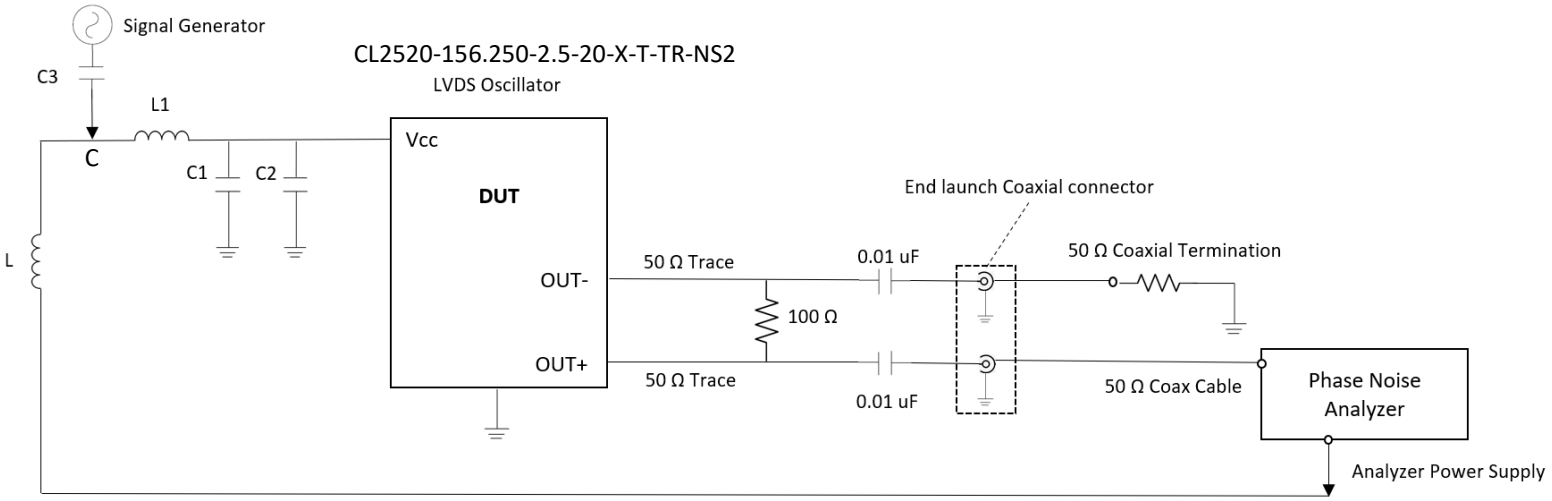
Raltron LVDS Oscillators Power Supply Noise Rejection Circuit Configurations

Circuit Configuration 2
Ferrite Choke and By-Pass Capacitors

Test equipment: Phase Noise Analyzer Agilent E5052B, Signal Generator Agilent 33250A.
Condition: Vdd=3.3V.

An AC sinewave signal is injected into the circuit at the point C indicated below and the waveform amplitude is measured to be 100mV at the Vin pin of the LDO. The signal frequency is sequentially modified from 10kHz to 100kHz, 1MHz and 10MHz respectively and phase noise is measured in each case. The measurements are made at room temp, utilizing the circuit below,

The following components values are recommended: C1=0.1uF, C2=0.01uF, C3=20.1uF, L1=1.5uH. The by-pass capacitors must be placed as close to Vcc & GND pins as possible. The inductor L1 is improving the circuit PSRR by acting as a low pass filter in connection with the other capacitors. The inductor L (L=4.7uH) is only part of the test fixture to prevent grounding of injected AC sinewave signal.



Offset Frequency from Fo	Fn =10kHz	Fn =100kHz	Fn =1 MHz	Fn =10 MHz
Phase Noise Spur Value Induced by Signal Generator [dBc/Hz]	-95.3	-122.56	-117.12	-156.30

RALTRON ELECTRONICS ▪ 10400 N.W. 33rd Street ▪ Miami, Florida 33172 ▪ U.S.A.
Telephone: +1-305-593-6033 ▪ Fax: +1-305-594-3973 ▪ e-mail: sales@raltron.com ▪ internet: http://www.raltron.com

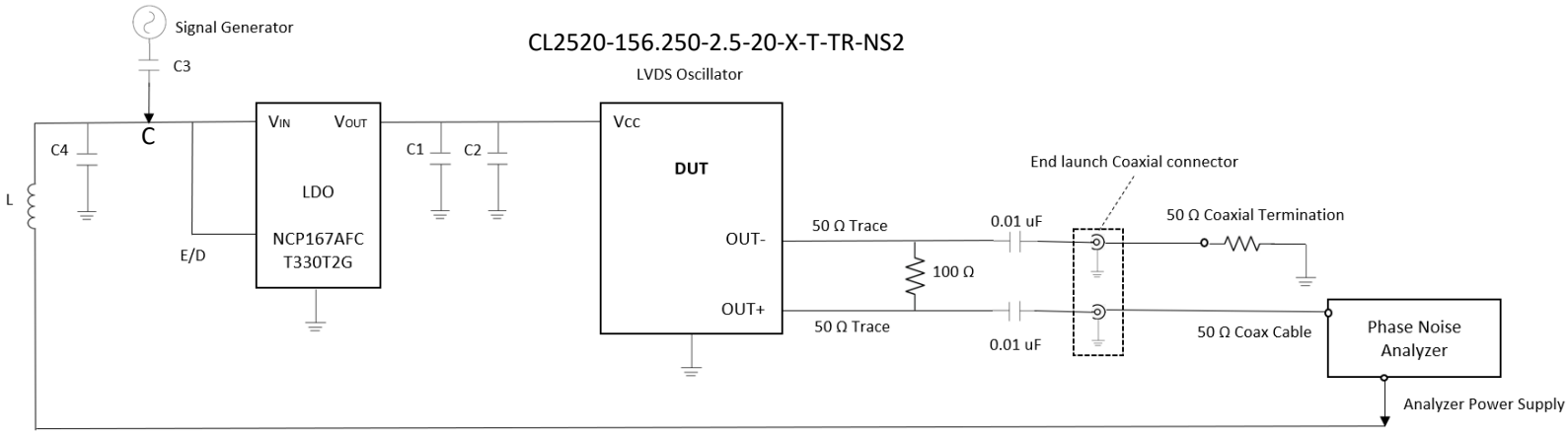
Raltron LVDS Oscillators Power Supply Noise Rejection Circuit Configurations

Circuit Configuration 3
LDO and By-Pass Capacitors

Test equipment: Phase Noise Analyzer Agilent E5052B, Signal Generator Agilent 33250A.
Condition: Vdd=3.3V.

An AC sinewave signal is injected into the circuit at the point C indicated below and the waveform amplitude is measured to be 100mV at the Vin pin of the LDO. The signal frequency is sequentially modified from 10kHz to 100kHz, 1MHz and 10MHz respectively and phase noise is measured in each case. The measurements are made at room temp, utilizing the circuit below,

The following components values are recommended: C1=1uF, C2=0.1uF, C3=20.1uF, C4=1uF. The by-pass capacitors must be placed as close to Vcc & GND pins as possible. The inductor L (L=4.7uH) is only part of the test fixture to prevent grounding of injected AC sinewave signal. The use of an LDO (Low Dropout Regulator) between the on-board power supply output and the oscillator Vcc pin is recommended. The ON Semiconductor LDO P.N. CNP167AFCT330T2G has been successfully tested for this purpose. The LDO performance is superior to the performance of filters used in the previous solutions.



Offset Frequency from Fo	Fn =10kHz	Fn =100kHz	Fn =1 MHz	Fn =10 MHz
Phase Noise Spur Value Induced by Signal Generator [dBc/Hz]	-145.20	-153.50	-158.10	-160.00

RALTRON ELECTRONICS ▪ 10400 N.W. 33rd Street ▪ Miami, Florida 33172 ▪ U.S.A.
Telephone: +1-305-593-6033 ▪ Fax: +1-305-594-3973 ▪ e-mail: sales@raltron.com ▪ internet: http://www.raltron.com

Raltron LVDS Oscillators Power Supply Noise Rejection Circuit Configurations

Comparison Between the Three Proposed Circuit Configurations

Solutions	Recommended Components	Parameter	CL2520-156.250-2.5-20-X-T-TR-NS2			
		Frequency Offset from Fo	Fn =10kHz	Fn =100kHz	Fn =1 MHz	Fn =10 MHz
#1 By-pass capacitors	0201 Caps: 0.6x0.3x0.3mm	Phase Noise Spur Amplitude [dBc/Hz] Induced by Input Sinewave Signal of 100 mV	-94.60	-120.56	-103.77	-148.18
#2 Ferrite Choke and by-pass capacitors	Ferrite Choke: 1.7x0.9x0.9mm 0201 Caps: 0.6x0.3x0.3mm		-95.30	-122.56	-117.12	-156.30
#3 LDO and by-pass capacitors	LDO PN. ON SEMI NCP167AFCT330T2G: 0.65x0.65x0.33mm 0201 Caps: 0.6x0.3x0.3mm		-145.20	-153.50	-158.10	-160.00

Recommendation

Raltron LVDS oscillators show an excellent intrinsic PSRR, however for increased performance the use of an LDO is recommended.

ON SEMI LDO PN NCP167AFCT330T2G is offering a low- cost solution for an excellent PSRR and a very small size package compatible with the smallest sized applications (example QSFP-DD optical transceivers)
Datasheet: NCP167AFCT330T2G

Circuit Configuration 3 is recommended for optimum PSRR/size/cost performance.

RALTRON ELECTRONICS ▪ 10400 N.W. 33rd Street ▪ Miami, Florida 33172 ▪ U.S.A.
Telephone: +1-305-593-6033 ▪ Fax: +1-305-594-3973 ▪ e-mail: sales@raltron.com ▪ internet: http://www.raltron.com