AN2867
Application note

Oscillator design guide for STM8S, STM8A and STM32 microcontrollers

Introduction

Most designers are familiar with oscillators (Pierce-Gate topology), but few really understand how they operate, let alone how to properly design an oscillator. In practice, most designers do not even really pay attention to the oscillator design until they realize the oscillator does not operate properly (usually when it is already being produced). This should not happen. Many systems or projects are delayed in their deployment because of a crystal not working as intended. The oscillator should receive its proper amount of attention during the design phase, well before the manufacturing phase. The designer would then avoid the nightmare scenario of products being returned.

This application note introduces the Pierce oscillator basics and provides some guidelines for a good oscillator design. It also shows how to determine the different external components and provides guidelines for a good PCB for the oscillator.
This document finally contains an easy guideline to select suitable crystals and external components, and it lists some recommended crystals (HSE and LSE) for STM32 and STM8A/S microcontrollers in order to quick start development. Refer to *Table 1* for the list of applicable products.

Table 1. Applicable products

Type	Product categories
Microcontrollers	STM8S Series
	STM8AF Series, STM8AL Series
	STM32 32-bit ARM Cortex MCUs.

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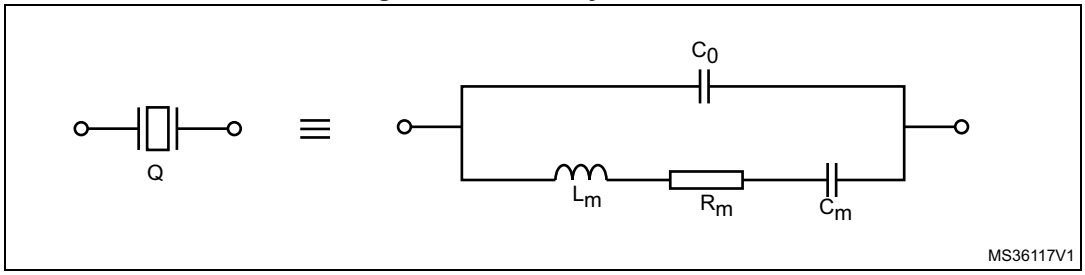
1 Quartz crystal properties and model

A quartz crystal is a piezoelectric device transforming electric energy to mechanical energy and vice versa. The transformation occurs at the resonant frequency. The quartz crystal can be modeled as follows:

Figure 1. Quartz crystal model



C_0: represents the shunt capacitance resulting from the capacitor formed by the electrodes

L_m: (motional inductance) represents the vibrating mass of the crystal

C_m: (motional capacitance) represents the elasticity of the crystal

R_m: (motional resistance) represents the circuit losses

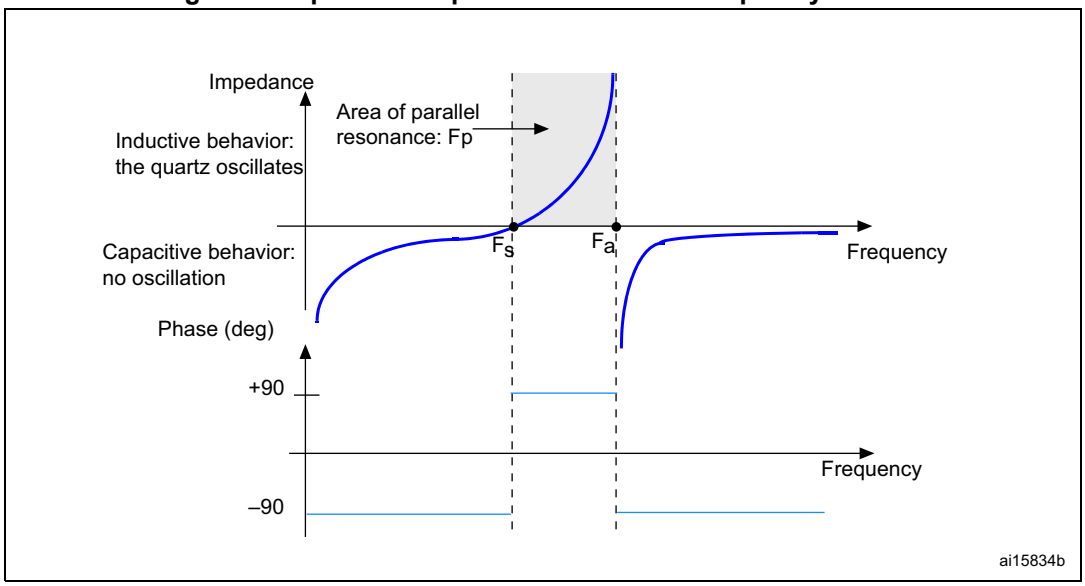
The impedance of the crystal is given by the following equation (assuming that R_m is negligible):

(1)

$$Z = \frac{j}{w} \times \frac{w^2 \times L_m \times C_m - 1}{(C_0 + C_m) - w^2 \times L_m \times C_m \times C_0}$$

Figure 2 represents the impedance in the frequency domain.

Figure 2. Impedance representation in the frequency domain



F_s is the series resonant frequency when the impedance Z = 0. Its expression can be deduced from equation (1) as follows:

(2)

$$F_s = \frac{1}{2\pi\sqrt{L_m C_m}}$$

F_a is the anti-resonant frequency when impedance Z tends to infinity. Using equation (1), it is expressed as follows:

(3)

$$F_a = F_s\sqrt{1 + \frac{C_m}{C_0}}$$

The region delimited by F_s and F_a is usually called the area of parallel resonance (shaded area in *Figure 2*). In this region, the crystal operates in parallel resonance and behaves as an inductance that adds an additional phase equal to 180 ° in the loop. Its frequency F_p (or F_L: load frequency) has the following expression:

(4)

$$F_p = F_s\left(1 + \frac{C_m}{2(C_0 + C_L)}\right)$$

From equation (4), it appears that the oscillation frequency of the crystal can be tuned by varying C_L load capacitance. This is why in their datasheets, crystal manufacturers indicate the exact C_L required to make the crystal oscillate at the nominal frequency.

Table 2 gives an example of equivalent crystal circuit component values to have a nominal frequency of 8 MHz.

Table 2. Example of equivalent circuit parameters

Equivalent component	Value
R_m	8 Ω
L_m	14.7 mH
C_m	0.027 pF
C_0	5.57 pF

Using equations (2), (3) and (4) we can determine F_s, F_a and F_p of this crystal:

$F_s = 7988768\ \text{Hz}$ and $F_a = 8008102\ \text{Hz}$.

If the load capacitance C_L at the crystal electrodes is equal to 10 pF, the crystal will oscillate at the following frequency: $F_p = 7995695\ \text{Hz}$.

To have an oscillation frequency of exactly 8 MHz, C_L should be equal to 4.02 pF.

2 Oscillator theory

Oscillators are one of the backbone components of modern digital ICs. They can be classified into different sub-families depending on their topology and operating principles. To each oscillator sub-family corresponds a more suitable mathematical model that can be used to study the oscillator behavior and theoretically determine its performance.

This section deals only with harmonic oscillators (relaxation oscillators are not within the scope of this application note) with a particular focus on Pierce-oscillator topology (see *Section 3: Pierce oscillator design* for details). This restricted scope is due to the fact that all the oscillators embedded in STM32 microcontrollers covered by this document that require external passive components (external resonator, load capacitors, etc.) are of the previously mentioned type and topology.

The harmonic oscillator family can be divided into two main sub-families:

- Negative-resistance oscillators
- Positive-feedback oscillators.

These two sub-families of oscillators are similar for what regards the output waveform. They deliver an oscillating waveform at the desired frequency. This waveform is typically composed of a fundamental sine-waveform at the desired frequency plus a sum of overtone harmonics (at frequencies multiple of the fundamental one) due to the nonlinearity of some components of the oscillation loop.

These two sub-families differ in their operating principles. This difference also implies a different mathematical model to describe and analyze each sub-family.

Positive-feedback oscillators are generally modeled using the famous Barkhausen model where an oscillator should fulfill the Barkhausen criterion to be able to maintain a stable oscillation at the desired frequency.

Negative-resistance oscillators could be described by the Barkhausen model. However this approach is not adequate. The most suitable approach to analyze a negative-resistance oscillator is by using the negative-resistance model as described in E. Vittoz's paper (*[1]*).

Since STM32 low-speed external (LSE) oscillator and high-speed external (HSE) oscillators were both designed following the negative-resistance principle, this section focuses on the presentation of the negative-resistance model.

2.1 Negative resistance

Theoretically speaking, a negative resistance would be a dipole that absorbs heat and converts the energy into an electrical current proportional to the applied voltage but flowing in the opposite direction (exactly the opposite mechanism of an electrical resistance). In the real word such a dipole does not exist.

In fact the term "negative resistance" is a misnomer of the "negative transresistance" which is defined by the ratio of a given voltage variation (ΔV) divided by the induced current variation (ΔI). Unlike the resistance which is always positive, the transresistance (also known as differential resistance) can be either positive or negative. *Figure 3* gives the current-voltage curve for a dipole that shows a negative transresistance region. It is obvious that the V/I ratio is always positive. However this is not the case for the $\Delta V/\Delta I$ ratio.

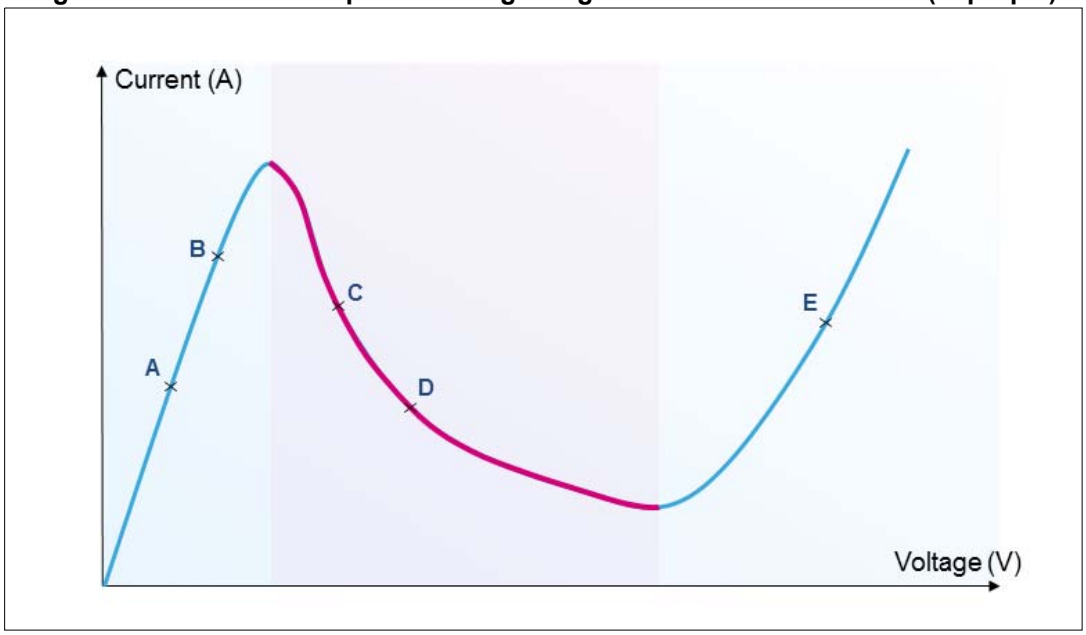
The part of the I-V curve represented in purple shows a negative transresistance:

$$\frac{\Delta V}{\Delta I} = \frac{V(D) - V(C)}{I(D) - I(C)} < 0$$

while the parts of the curve in blue shows a positive transresistance:

$$\frac{\Delta V}{\Delta I} = \frac{V(B) - V(A)}{I(B) - I(A)} > 0$$

Figure 3. I-V curve of a dipole showing a negative transresistance area (in purple)



2.2 Transconductance

Like the conductance which is defined as the inverse of the resistance, the transconductance is also defined as the inverse of the transresistance. Transconductance can also be defined as the differential conductance which expressed by the formula:

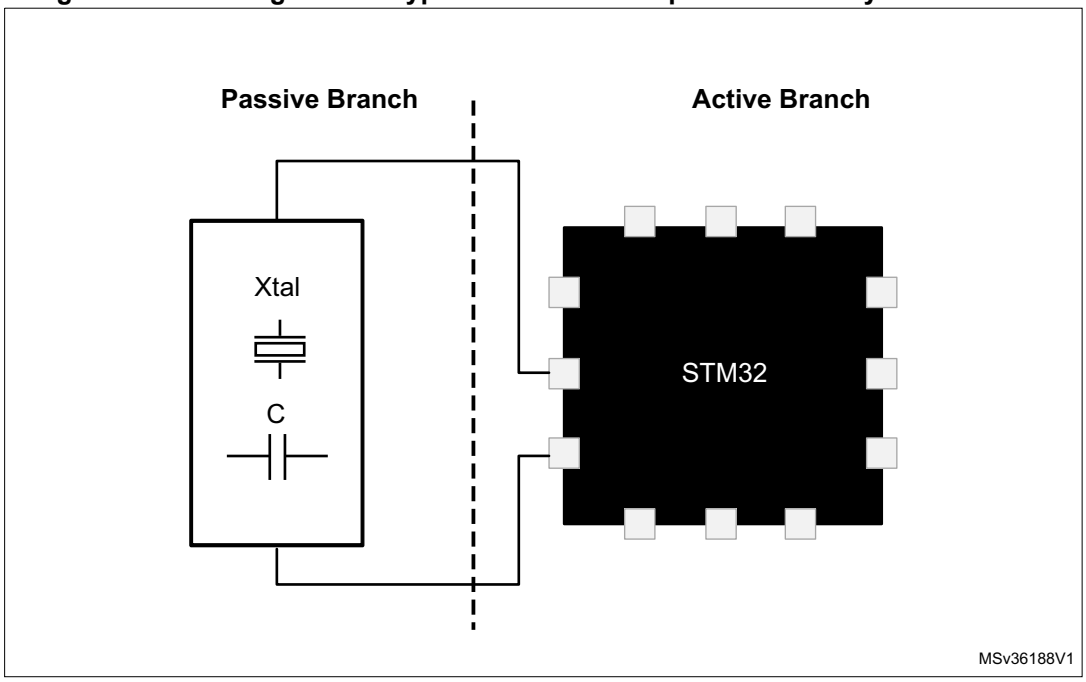
$$\frac{\Delta V}{\Delta I}$$

2.3 Negative-resistance oscillator principles

An oscillation loop is made of two branches (see *Figure 4*):

- The active branch of the oscillation loop which is composed of the oscillator itself. This branch is responsible for providing enough energy at startup to make the oscillation start and build up until it reaches the stable oscillation phase. When a stable oscillation is reached, the oscillator branch provides enough energy to compensate for the oscillation loop passive branch losses.
- The passive branch is mainly composed of the resonator, the two load capacitors and all the parasitic capacitances.

Figure 4. Block diagram of a typical oscillation loop based on a crystal resonator



Following the small signals theory and when the active branch (oscillator part) is correctly biased, the latter should have its transconductance equal to the passive branch conductance in order to maintain a stable oscillation around the oscillator biasing voltage.

However, at startup, the oscillator transconductance should be higher than (multiple of) the conductance of the passive part of the oscillation loop to maximize the possibility to build up the oscillation from inherent noise of the oscillation loop. Please note that an excessive oscillator transconductance compared to the oscillation loop passive branch conductance may also saturate the oscillation loop and cause a startup failure.

In order to ensure the oscillator ability to startup successfully and maintain stable oscillation, a ratio between the negative resistance of the oscillation loop and the crystal maximal equivalent series resistance (ESR) is specified: for STM32 and STM8 microcontrollers, it is recommended to have a ratio higher than x5 for the HSE oscillators and higher than x3 for the LSE oscillators.

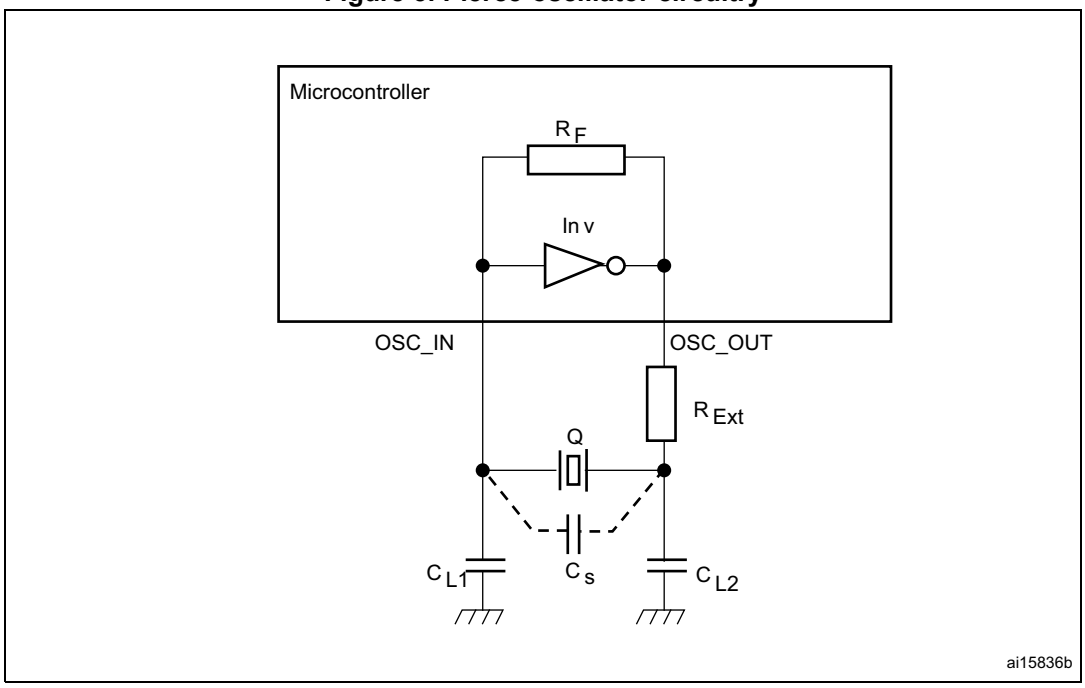
3 Pierce oscillator design

This section describes the different parameters and how to determine their values in order to be compliant with the Pierce oscillator design.

3.1 Introduction to pierce oscillators

Pierce oscillators are variants of Colpitts oscillators which are widely used in conjunction with crystal resonators. A Pierce oscillator requires a reduced set of external components which results in a lower final design cost. In addition, the Pierce oscillator is known for its stable oscillation frequency when paired with a crystal resonator, in particular a quartz-crystal resonator.

Figure 5. Pierce-oscillator circuitry



Inv: the internal inverter that works as an amplifier

Q: crystal quartz or a ceramic resonator

R_F: internal feedback resistor

R_{Ext}: external resistor to limit the inverter output current

C_{L1} and C_{L2}: are the two external load capacitances

C_s: stray capacitance is the addition of the microcontroller pin capacitance (OSC_IN and OSC_OUT) and the PCB capacitance: it is a parasitic capacitance.

3.2 R_F feedback resistor

In most STMicroelectronics microcontrollers, R_F is embedded in the oscillator circuitry. Its role is to make the inverter act as an amplifier. The feedback resistor is connected between V_{in} and V_{out} so as to bias the amplifier at $V_{out} = V_{in}$ and force it to operate in the linear region (shaded area in *Figure 6*). The amplifier amplifies the noise (for example, the thermal noise of the crystal) within the range of serial to parallel frequency (F_a, F_a). This noise causes the oscillations to start up. In some cases, if R_F is removed after the oscillations have stabilized, the oscillator continues to operate normally.

Figure 6. Inverter transfer function

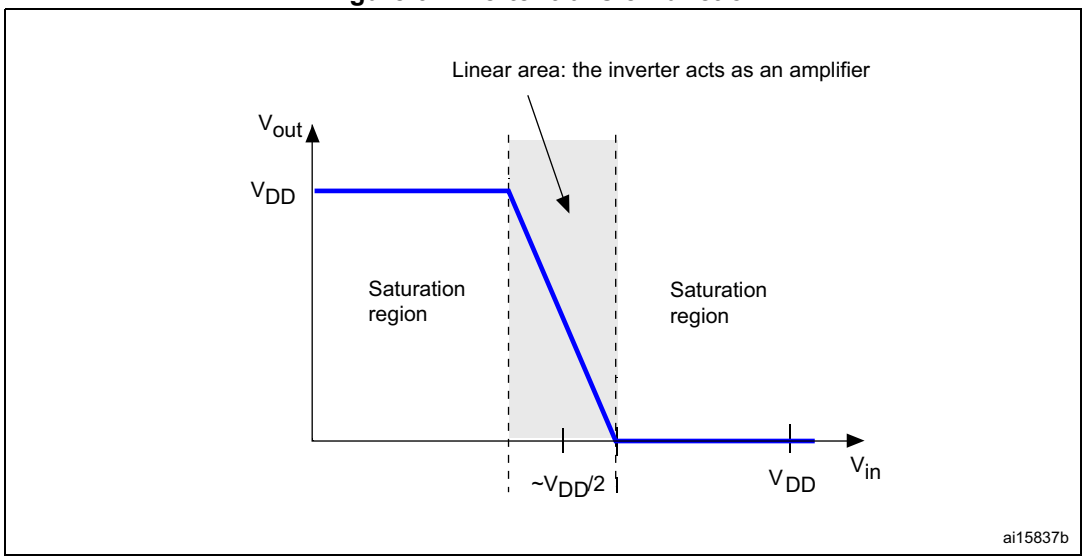


Table 3 provides typical values of R_F.

Table 3. Typical feedback resistor values for given frequencies

Frequency	Feedback resistor range
32.768 kHz	10 to 25 MΩ
1 MHz	5 to 10 MΩ
10 MHz	1 to 5 MΩ
20 MHz	470 kΩ to 5 MΩ

3.3 C_L load capacitance

The load capacitance is the terminal capacitance of the circuit connected to the crystal oscillator. This value is determined by the external capacitors C_{L1} and C_{L2} and the stray capacitance of the printed circuit board and connections (C_s). The C_L value is specified by the crystal manufacturer. Mainly, for the frequency to be accurate, the oscillator circuit has to show the same load capacitance to the crystal as the one the crystal was adjusted for. Frequency stability mainly requires that the load capacitance be constant. The external capacitors C_{L1} and C_{L2} are used to tune the desired value of C_L to reach the value specified by the crystal manufacturer.

The following equation gives the expression of C_L:

$$C_L = \frac{C_{L1} \times C_{L2}}{C_{L1} + C_{L2}} + C_s$$

Example of C_{L1} and C_{L2} calculation:

For example if the C_L value of the crystal is equal to 15 pF and, assuming that C_s = 5 pF, then:

$C_L - C_s = \frac{C_{L1} \times C_{L2}}{C_{L1} + C_{L2}} = 10\ pF$. That is: $C_{L1} = C_{L2} = 20\ pF$.

3.4 Oscillator transconductance

Theoretically, to make the oscillation start and build up until it reaches a stable oscillation phase, the oscillator should provide sufficient gain that at the same time compensates for the oscillation loop losses and provide the energy that makes the oscillation build up. When the oscillation becomes stable, the equality between the oscillator provided power and the oscillation loop dissipated power is achieved.

Practically speaking and due to tolerances on passive component values and their dependency on environmental parameters (e.g. temperature), a ratio of x1 between the oscillator gain and the oscillation loop critical gain is not recommended. This will induce a too long oscillator startup time and might even prevent the oscillator from starting up.

This section describes the two approaches that can be used to check if an STM32 oscillator can be paired with a given resonator in order to ensure that the oscillation is started and maintained under the specified conditions for both resonator and oscillator. The approach depends on how the oscillator parameters are specified in the microcontroller datasheet:

- If the oscillation loop maximal critical gain parameter ($g_{m\_crit\_max}$) is specified, it is important to make sure that the oscillation loop critical gain (g_{mcrit}) is smaller than the specified parameter.
- If the oscillator transconductance parameter (g_m) is specified, make sure that the gain margin ratio ($gain_{margin}$) is bigger than x5. Below the calculation formulas for both g_{mcrit} and $gain_{margin}$.

$$gain_{margin} = \frac{g_m}{g_{mcrit}}$$

where:

g_m is the oscillator transconductance specified in the microcontroller datasheet. Note that the HSE oscillator transconductance is in the range of a dozens of mA/V while LSE

oscillator transconductance ranges from a few µA/V to a few dozens of µA/V depending on the product.

g_{mcrit} is defined as the minimal transconductance of an oscillator required to maintain a stable oscillation when it is a part of the oscillation loop for which this parameter is relevant. g_{mcrit} is computed from oscillation-loop passive components parameters. Assuming that C_{L1} equals C_{L2}, and that the crystal sees the same C_L on its pads as the value given by the crystal manufacturer, g_{mcrit} is expressed as follows:

$$g_{mcrit} = 4 \times ESR \times (2\pi F)^2 \times (C_0 + C_L)^2$$

where

ESR = equivalent series resistance

C0 is the crystal shunt capacitance.

CL is the crystal nominal load capacitance.

F is the crystal nominal oscillation frequency.

For example, to design the oscillation loop for the HSE oscillator embedded into an STM32F1 microcontroller which a transconductance value (g_m) equal to 25 mA/V, we choose a quartz crystal from Fox, with the following characteristics:

frequency = 8 MHz

C_0 = 7 pF

C_L = 10 pF

ESR = 80 Ω .

To check if this crystal will oscillate with an STM32F1 microcontroller, let us calculate g_{mcrit}:

$$g_{mcrit} = 4 \times 80 \times (2 \times \pi \times 8 \times 10^6)^2 \times (7 \times 10^{-12} + 10 \times 10^{-12})^2 = 0{,}23 \text{ mA/V}$$

Calculating the gain margin gives:

$$gain_{margin} = \frac{g_m}{g_{mcrit}} = \frac{25}{0{,}23} = 107$$

The gain margin is sufficient to start the oscillation and the “gain margin greater than 5” condition is reached. The oscillator is expected to reach a stable oscillation after a typical delay specified by the microcontroller datasheet.

If an insufficient gain margin is found ($gain_{margin}$ < 5), the oscillation might start up under typical conditions (achieved in laboratory conditions) when designing and testing the final application. However, this does not guarantee that the oscillation will start up in operating conditions. As a result, it is highly recommended that the selected crystal has a gain margin higher than or equal to 5. Try to select a crystal with a lower ESR or/and a lower C_L.

Whatever the specified parameter, the oscillator transconductance (g_m) or the oscillation loop maximal critical gain ($g_{m\_crit\_max}$), the conversion between these two parameters is possible, if need be. The relation between these two parameters is given by the below formula:

$$G_{m\_crit\_max} = \frac{g_m}{5}$$

3.5 Drive level (DL) and external resistor (R_{Ext}) calculation

The drive level (DL) and external resistor value (R_{Ext}) are closely related and will be addressed in the same section.

3.5.1 Calculating drive level (DL)

The drive level is the power dissipated in the crystal. It has to be limited otherwise the quartz crystal can fail due to excessive mechanical vibration. The maximum drive level is specified by the crystal manufacturer, usually in mW. Exceeding this maximum value may lead to the crystal being damaged or to a shorter device lifetime.

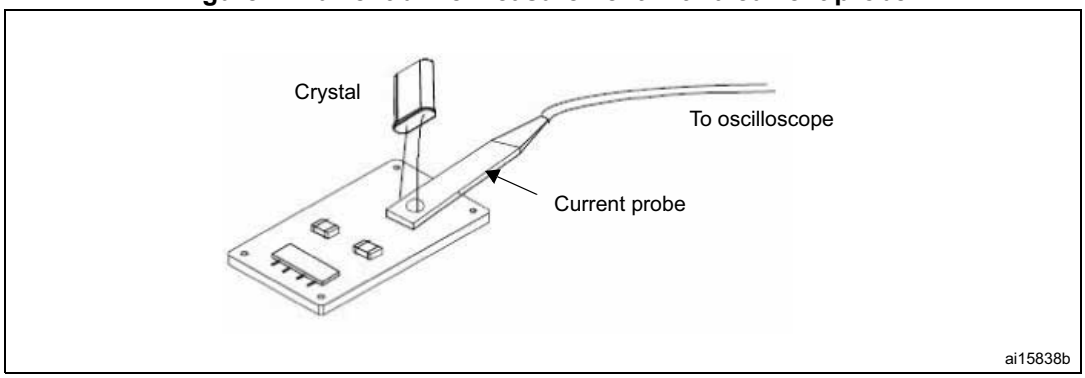
The drive level is given by the following formula: $DL = ESR \times I_Q^2$, where:

- ESR is the equivalent series resistor (specified by the crystal manufacturer):

$$ESR = R_m \times \left(1 + \frac{C_0}{C_L}\right)^2$$

- I_Q is the current flowing through the crystal in RMS. This current can be displayed on an oscilloscope as a sine wave. The current value can be read as the peak-to-peak value (I_{PP}). When using a current probe (as shown in *Figure 7*), the voltage scale of an oscilloscope may be converted into 1mA/1mV.

Figure 7. Current drive measurement with a current probe



So as described previously, when tuning the current with the potentiometer, the current through the crystal does not exceed $I_Q$max RMS (assuming that the current through the crystal is sinusoidal).

Thus $I_Q$max RMS is given by:

$$I_{Qmax}RMS = \sqrt{\frac{DL_{max}}{ESR}} = \frac{I_{Qmax}PP}{2\sqrt{2}}$$

Therefore the current through the crystal (peak-to-peak value read on the oscilloscope) should not exceed a maximum peak-to-peak current (I_{Qmax}PP) equal to:

$$I_{Qmax}PP = 2 \times \sqrt{\frac{2 \times DL_{max}}{ESR}}$$

Hence the need for an external resistor (R_{Ext}) (refer to *Section 3.5.3*) when I_Q exceeds I_{Qmax}PP. The addition of R_{Ext} then becomes mandatory and it is added to ESR in the expression of I_{Qmax}.

3.5.2 Another drive level measurement method

The drive level can be computed as:
DL= I^2_{QRMS} × ESR, where I_{QRMS} is the RMS AC current.

This current can be calculated by measuring the voltage swing at the amplifier input with a low-capacitance oscilloscope probe (no more than 1 pF). The amplifier input current is negligible with respect to the current through C_{L1}, so we can assume that the current through the crystal is equal to the current flowing through C_{L1}. Therefore the RMS voltage at this point is related to the RMS current by:

$I_{QRMS} = 2\pi F \times V_{RMS} \times C_{tot}$, with:

- F = crystal frequency
- $V_{RMS} = \frac{V_{pp}}{2\sqrt{2}}$, where: V_{pp} is the voltage peak-to-peak measured at C_{L1} level
- $C_{tot} = C_{L1} + (C_s/2) + C_{probe}$ where:
  - C_{L1} is the external load capacitance at the amplifier input
  - C_s is the stray capacitance
  - C_{probe} is the probe capacitance)

Therefore the drive level, DL, is given by: $DL = \frac{ESR \times (\pi \times F \times C_{tot})^2 \times (V_{pp})^2}{2}$.

This DL value must not exceed the drive level specified by the crystal manufacturer.

3.5.3 Calculating external resistor (R_{Ext})

The role of this resistor is to limit the drive level of the crystal. With C_{L2}, it forms a low-pass filter that forces the oscillator to start at the fundamental frequency and not at overtones (prevents the oscillator from vibrating at 3, 5, 7 etc. times the fundamental frequency). If the power dissipated in the crystal is higher than the value specified by the crystal manufacturer, the external resistor R_{Ext} becomes mandatory to avoid overdriving the crystal. If the power dissipated in the selected quartz is less than the drive level specified by the crystal manufacturer, the insertion of R_{Ext} is not recommended and its value is then 0 Ω.

An initial estimation of R_{Ext} is obtained by considering the voltage divider formed by R_{Ext}/C_{L2}. Thus, the value of R_{Ext} is equal to the reactance of C_{L2}.

Therefore: $R_{Ext} = \frac{1}{2\pi F C_2}$.

Let us put:

- oscillation frequency F = 8 MHz
- C_{L2} = 15 pF

Then: R_{Ext} = 1326 Ω

The recommended way of optimizing R_{Ext} is to first choose C_{L1} and C_{L2} as explained earlier and to connect a potentiometer in the place of R_{Ext}. The potentiometer should be initially set to be approximately equal to the capacitive reactance of C_{L2}. It should then be adjusted as required until an acceptable output and crystal drive level are obtained.

Caution: After calculating R_{Ext} it is recommended to recalculate the gain margin (refer to *Section 3.4: Oscillator transconductance*) to make sure that the addition of R_{Ext} has no effect on the oscillation condition. That is, the value of R_{Ext} has to be added to ESR in the expression of g_{mcrit} and $g_m >> g_{mcrit}$ must also remain true:

$g_m >> g_{mcrit} = 4 \times (ESR + R_{Ext}) \times (2 \times PI \times F)^2 \times (C_0 + C_L)^2$

Note: If R_{Ext} is too low, there is no power dissipation in the crystal. If R_{Ext} is too high, there is no oscillation: the oscillation condition is not reached.

3.6 Startup time

The startup time is the time required by the oscillation to start up and then build up until it reaches a stable oscillation phase. The startup time depends, among other factors, on the Q-factor of the resonator used. If the oscillator is paired with a quartz-crystal resonator characterized by its high Q-factor then the startup time will be higher if a ceramic resonator is used (ceramic resonators are know for their poor Q-factor compared to quartz-crystal resonators). The startup time also depends on the external components, C_{L1} and C_{L2}, and on the crystal frequency. The higher the crystal nominal frequency, the lower the start up time. In addition the startup problems are usually due to the fact that the gain margin is not properly dimensioned (as explained previously). This is caused either by C_{L1} and C_{L2} being too small or too large, or by the ESR being too high.

As an example, an oscillator paired with a few-MHz nominal frequency crystal resonator would typically start up after a delay of few ms.

The startup time of a 32.768 kHz crystal ranges from 1 to 5 s.

3.7 Crystal pullability

Crystal pullabilty, also known as crystal sensitivity, measures the impact of small variations of the load capacitance seen by the crystal on the oscillation frequency shifting. This parameter usually has more importance when dealing with low-speed oscillators, since they are used to clock time-keeping functions (such as real-time clock functions).

When the final application is still in design stage, the influence of this parameter on the low-speed oscillator accuracy (and consequently on all the time-keeping functions clocked by this oscillator) is not so obvious. This is due to the fact that the designer fine tunes the load capacitors until the desired oscillation frequency is obtained. When the design reaches production stage. it is frozen and all the passive components including the load capacitors have their values well defined. Any change of the load capacitance will directly induce a shift of the oscillation frequency. Changes in the capacitive load (C_L) seen by the crystal may be thought of as due to inadequate operation environment and only happening when the final design is not properly operated. In practice, this is not true since changes of the load capacitance are rather frequent and must by taken into account by the designer. The main contributors to the capacitive load (C_L) seen by the oscillator are the following:

- The capacitance of the load capacitors C_{L1} and C_{L2}
- The stray capacitance of the PCB paths
- The parasitic capacitance of the oscillator pins.

Any change on the capacitances listed above directly shifts the oscillation frequency. When the design is in production stage, many of these capacitance values cannot be accurately controlled. Selecting a crystal with low-pullability will limit the influence of such production uncertainties on the final oscillation frequency accuracy.

Generally speaking, the higher the load capacitance (C_L) of a crystal, the lower its pullability. As an example, let us consider a crystal with a pullability of 45 PPM/pF. To fine tune the oscillation frequency, this crystal is loaded by two C0G ceramic capacitors, C_{L1} and C_{L2}, with equal capacitances equal to 7 pF. C0G ceramic capacitors have a tolerance value of

± 5% of their nominal value. From crystal point of view, the two load capacitors are mounted in series which means that their contribution to the C_L is (C_{L1} = C_{L2})/2. As C_{L1} equals C_{L2}, the tolerance on their contribution to C_L remains the same and is equal to ± 5%. Now if we consider that all the remaining contributors to the C_L are maintained to their nominal values at design stage (to assess the frequency shift magnitude induced only by load capacitor tolerances), then the load capacitance seen by the crystal (C_L) will either decrease by 0.175 pF or increase by the same value. This will induce an oscillation shift of:

$0.175\ pF \times 45\ PPM/pF = \sim 7.8\ PPM$ (~0.7 s/day for a time-keeping function such as RTC)

The above example shows that the lower the pullability, the lower the impact of small load capacitance deviation on the frequency shifting. Crystal pullability is an important factor when defining the final application PPM budget.

$$Pullability_{(PPM/pF)} = \frac{C_m \times 10^6}{2 \times (C_0 + C_L)^2}$$

Where

C_m is the crystal motional capacitance

C_0 is the crystal shunt capacitance

C_L is the crystal nominal load capacitance

Next sections give a more detailed description on how to calibrate the oscillation frequency and how to estimate the final accuracy uncertainty (PPM) budget.

3.8 Safety factor

3.8.1 Definition

Resonators (such as crystal resonators) are well known to undergo aging effects. They manifest themselves over time in a deviation of resonator parameters from their initial values defined by the resonator specifications. Among the affected parameters there is the resonator ESR which value depends on the surrounding environmental conditions such as moisture and temperature.

The oscillator transconductance also depends on the microcontroller power supply voltage and on the temperature.

The safety factor parameter allows to qualify the oscillator safe operation under the operating conditions and during the application life. It measures the ability of the oscillator not to fail under operating conditions.

The safety factor is defined as the ratio between the oscillator negative resistance and the resonator ESR. It is given by the below formula:

$$S_f = \frac{\text{Oscillator negative resistance}}{\text{Crystal ESR}} = \frac{R_{ADD} + \text{Crystal ESR}}{\text{Crystal ESR}}$$

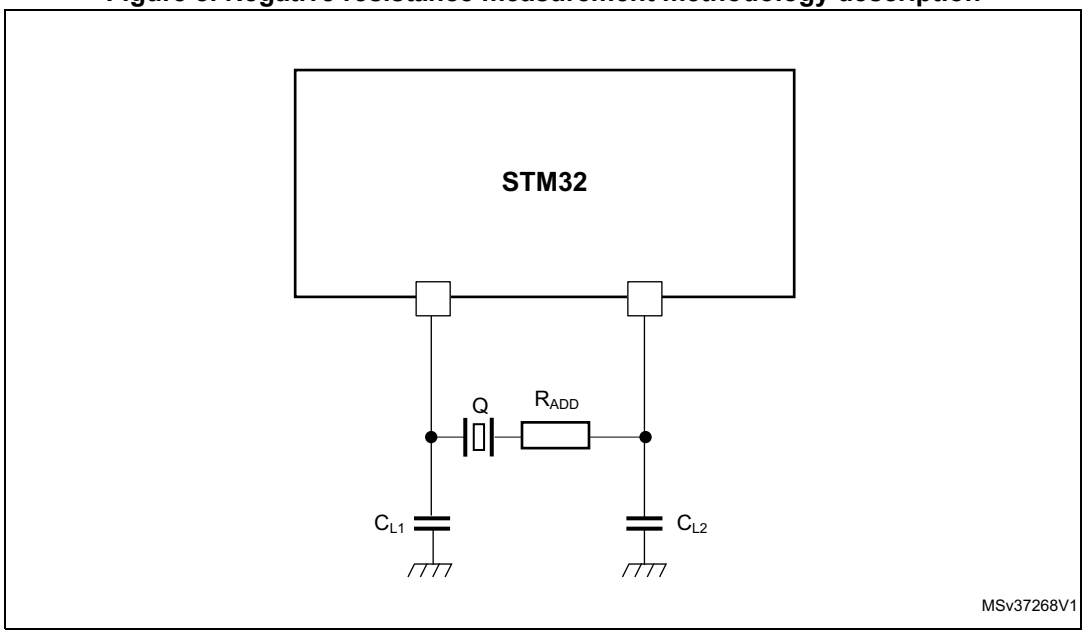
3.8.2 Measurement methodology

To measure the oscillator negative resistance, a resistance is added in series with the resonator as described in *Figure 8*.

The oscillator negative resistance is the value of smallest series resistance that will prevent the oscillator from starting up successfully.

In practice, this is achieved by conducting several experiments in which the value of the series resistance is slightly increased compared to the previous experiment. This sequence of experiments should stop when the oscillator is not able to start up correctly. This allows determining the oscillator negative resistance which is equal to the value of the added series resistance.

Figure 8. Negative resistance measurement methodology description



3.8.3 Safety factor for STM32 and STM8 oscillators

Table 4 gives a summary of the safety factors for the oscillators embedded in STM32 and STM8 microcontrollers. It should be noted that for the LSE oscillator, the oscillation is considered safe for a safety factor higher than or equal to x3, while for the HSE oscillator, the oscillation is considered safe starting from a safety factor higher than or equal to x5.

Table 4. Safety Factor (S_f) for STM32 and STM8 oscillators(1)

Safety Factor (S_f)	Assurance level	
	HSE	LSE
$S_f \geq 5$	Safe	Very Safe
$3 \leq S_f < 5$	Not Safe	Safe
$S_f < 3$		Not Safe

1. Safe and very safe oscillations are shown in green while not safe oscillation is show in orange.

4 Guidelines for selecting suitable crystal and external components

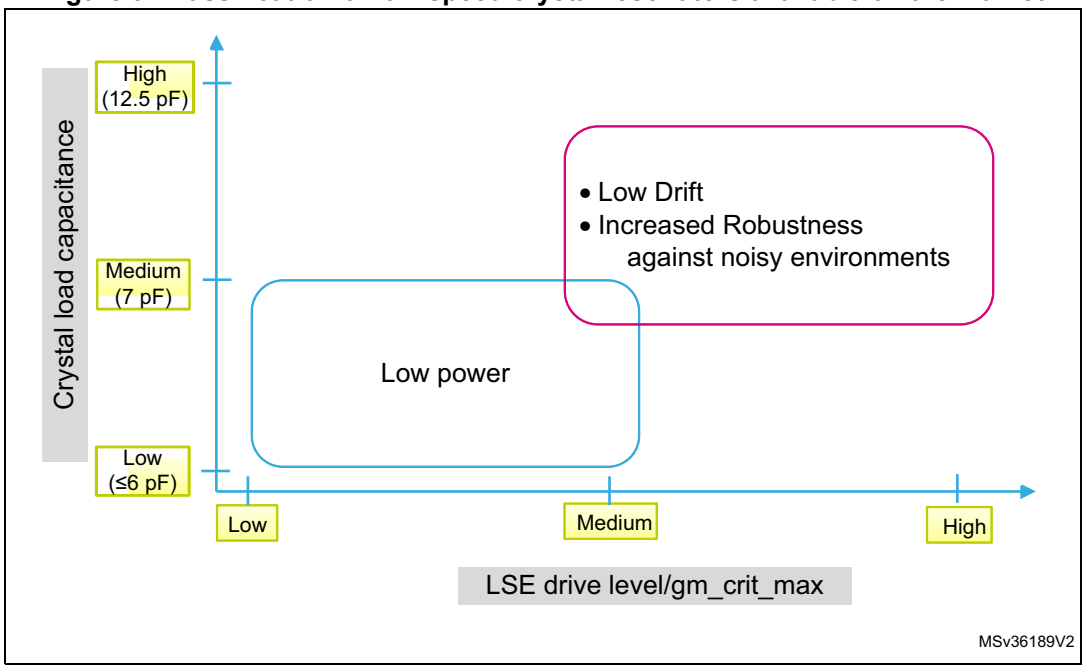
4.1 Low-speed oscillators embedded into STM32 microcontrollers

The low-speed resonator market provides a wide range of crystal resonators. Selecting the most adequate one for a given design depends on many parameters. Below a list of the most important parameters that must be taken into account (only technical factors are listed):

- Crystal size or footprint
- Crystal load capacitance (C_L)
- Oscillation frequency offset (PPM)
- Startup time.

A trade-off between the above parameters must be found depending on the key design criteria. *Figure 9* shows that the resonators available on the market can be divided into two categories depending on the above mentioned factors and trade-offs.

Figure 9. Classification of low-speed crystal resonators available on the market



A resonator with a relatively big load-capacitance (such as 12.5 pF) will require more power for the oscillator to drive the oscillation loop at the resonator nominal frequency. Designs targeting low-power consumption (e.g. RTC application powered by coin-batteries requiring very long autonomy) are consequently more likely to use resonators with relatively small load capacitance. On the other side, big load capacitance resonators have a much smaller pullabilty compared to resonators with small load capacitance. As a result, designs without severe constraints on power consumption tend to use big load capacitance crystals to reduce pullability.

One of the key emerging areas where crystal resonators are massively used is the handheld wearable appliance consumer market (e.g. smart phones, Bluetooth kits). For this market segment the crystal size is of critical importance. However it is widely known that small-footprint crystals come always with high crystal ESR. For this kind of designs, the choice may be harder if the target design has severe constraints in terms of power consumption (which almost always happens). In this case, choose a crystal with a load capacitance as small as possible to optimize power consumption even if this compromises pullabilty. In addition, crystals with high ESR may have a slightly longer startup time. If there are no constraints on crystal size, then it is recommended to choose a crystal with an ESR as small as possible.

In noisy environment (which it is almost always the case for industrial applications), if there are no constraints on power consumption, it is recommended to choose crystals with high load capacitance. These crystals will require a high-drive current from the oscillator while being more robust against noise and external perturbations. Another advantage is that the design pullability will be minimized.

Depending on which STM32 microcontroller is used, all the resonator families listed below can be compatible with your design or only some of them. STM32 microcontrollers embed two types of low-speed oscillator (LSE):

- Constant-gain low-speed oscillators

  This type of LSE oscillators features a constant gain which makes them compatible only with a few crystal groups mentioned above. For example, LSE oscillators embedded into STM32F2 and STM32L1 microcontrollers target designs with severe power consumption constraint. The selected crystal should consequently have a low load capacitance and a moderate ESR. LSE oscillators embedded into STM32F1 microcontrollers target crystal resonators with moderate ESR and moderate load capacitance.
- Configurable-gain low-speed oscillators

  LSE oscillators belonging to this family have the main advantage to be compatible with a large number of crystals. Almost no constraint will be induced by the STM32 microcontroller embedding this kind of LSE oscillator. This large list of compatible resonator crystals allows to focus only on design constraints (e.g. power consumption, footprint) when selecting a compatible resonator. These LSE oscillators are divided into two categories:
  - Dynamically (on-the-fly) modifiable gain LSE oscillators

    The gain of this type of LSE oscillators can be changed either before starting the oscillator or after enabling it.
  - Statically modifiable gain LSE oscillators

    The gain can be changed only when the LSE oscillator is turned off. If the oscillator transconductance has to be increased or decreased, the LSE must be turned off first.

Table 5 gives the list of low-speed oscillators (LSE) embedded into the STM32 microcontrollers.

Caution: When the gain is modified either statically or on-the-fly, the calibration of the oscillation frequency must be re-adjusted to estimate the final accuracy uncertainty (PPM) budget.

Caution: In STM32F0 and STM32F3 MCUs, High drive mode ($g_{m\_crit\_max}$ = 5 µA/V) should be used only with 12.5 pF crystals to avoid saturating the oscillation loop and causing a startup failure. When used with a low C_L crystal (eg C_L=6 pF), the oscillation frequency jitter and duty cycle may be distorted.

For simplification purposes, the following terms will be used in *Table 5: LSE oscillators embedded into STM32 microcontrollers*:

- F4_G1: STM32F4 series with LSE generation 1

  This category corresponds to STM32F401/405/ 407/427/429xx MCUs that feature LSE oscillators with non-modifiable transconductance
- F4_G2: STM32F4 series with LSE generation 2

  This category corresponds to STM32F411/446/469/479xx that feature LSE oscillators with statically-modifiable transconductance.

Table 5. LSE oscillators embedded into STM32 microcontrollers(1)

Drive-level	STM32F0/F3				STM32F1/T	STM32F2	F4_G1	F4_G2		STM32L0/L4				STM32L1	STM32F7				Unit
	Low	Medium Low	Medium High	High	NA	NA	NA	Low	High	Low	Medium Low	Medium High	High	NA	Low	Medium Low	Medium high	High	
g_{m_min}	5	8	15	25	5	2.8	2.8	2.8	7.5	2.5	3.75	8.5	13.5	3	2.4	3.75	8.5	13.5	µA/V
$g_{m\_crit\_max}$	1	1.6	3	5	1	0.56	0.56	0.56	1.5	0.5	0.75	1.7	2.7	0.6	0.48	0.75	1.7	2.7	

1. Color code:
   Blue: LSE oscillators with transconductance modifiable on the fly (dynamically).
   Green: LSE oscillators with non-modifiable transconductance.
   Gray: LSE oscillators with statically-modifiable transconductance.

4.2 Detailed steps to select an STM32-compatible crystal

This section describes the procedure recommended to select suitable crystal/external components. The whole procedure is divided into three main steps:

Step 1: Check the resonator compatibility with the selected STM32 microcontroller

To check the compatibility between the selected crystal and the STM32 microcontroller, first identify which procedure has to be followed among the two procedures described in *Section 3.4: Oscillator transconductance*. The decision should be made based on the oscillator specification provided in the product datasheet:

- If the oscillator transconductance parameter is specified, then the first procedure should be applied. Ensure that the gain margin ratio is higher than five (x5) to make sure that the crystal is compatible with the selected STM32 microcontroller.
- If $G_{m\_Crit\_max}$ is specified instead, make sure G_{m_crit} for the oscillation loop is smaller than the specified $G_{m\_Crit\_max}$ value.

Step 2: Determine the capacitance value of the load capacitors CL1 and CL2

To determine the right capacitance values for C_{L1} and C_{L2} load capacitors, apply the formula specified in *Section 3.3: CL load capacitance*. The values obtained are approximations of the exact capacitances to be used. In a second phase, to fine tune the values of the load capacitors, a series of experimental iterations should be performed until the right capacitance values are found.

During the experimental phase, use an etalon crystal. An etalon crystal is a characterized crystal which PPM drift is well known when it is loaded by the crystal nominal load capacitance (C_L). This kind of crystals can be provided by the crystal manufacturer upon request. After the etalon crystal has been chosen, calculate its oscillation frequency (F_{etalon}) when the crystal is loaded by its nominal load capacitance. This frequency is given by the formula:

$$F_{etalon} = F_{nominal} \times \left(PPM_{etalon} / 10^6 \right)$$

where:

F_{etalon} is the etalon crystal oscillation frequency when the crystal is loaded by its nominal load capacitance.

$F_{nominal}$ is the oscillation nominal frequency specified in the crystal datasheet.

PPM_{etalon} is the oscillation frequency drift of the etalon crystal as it was characterized by the crystal manufacturer.

When F_{etalon} is computed, execute the sequence below:

1. The first experimental iteration should be made with C_{L1} and C_{L2} capacitance values determined by calculation:
   - If the oscillation frequency is equal to F_{etalon}, then C_{L1} and C_{L2} are the correct capacitances. You can therefore skip sub-steps 2) and 3).
   - If the oscillation frequency is slower than F_{etalon} then go to sub-step 2).
   - Otherwise execute sub-step 3).
2. For this experimental iteration, decrease C_{L1} and C_{L2} capacitance values, measure again the oscillation frequency and compare it to F_{etalon}:
   - If the oscillation frequency is slower than F_{etalon}, execute sub-step 2).
   - Otherwise execute sub-step 3).
   - If the oscillation frequency is almost equal to F_{etalon} then the latter C_{L1} and C_{L2} capacitance values should be used.
3. For this experimental iteration, increase C_{L1} and C_{L2} capacitance values, measure again the oscillation frequency and compare it to F_{etalon}:
   - If the oscillation frequency is slower than F_{etalon} then execute sub-step 2).
   - Otherwise execute sub-step 3).
   - If the oscillation frequency is almost equal to F_{etalon} then the latter C_{L1} and C_{L2} capacitance values should be used.

Step 3: Check the Safety Factor of the oscillation loop

The safety factor should be assessed as described in *Section 3.8: Safety factor* to ensure a safe oscillation of the oscillator under operating conditions.

Note: Many crystal manufacturers can check microcontroller/crystal pairing compatibility upon request. If the pairing is judged valid, they can provide a report including the recommended C_{L1} and C_{L2} values as well as the oscillator negative resistance measurement. In this case steps 2 and 3 can be skipped.

Step 4: Calculate the drive level and external resistor

Compute the drive level (DL) (see *Section 3.5: Drive level (DL) and external resistor (REXt) calculation*) and check if it is greater or lower than $DL_{crystal}$:

- If $DL < DL_{crystal}$, no need for an external resistor. Congratulations you have found a suitable crystal.
- If $DL > DL_{crystal}$, you should calculate R_{Ext} in order to have: $DL < DL_{crystal}$. You should then recalculate the gain margin taking R_{Ext} into account.
  If you find that gain margin > 5, congratulations, you have found a suitable crystal. If not, then this crystal will not work and you have to choose another. Return to step 1 to run the procedure for the new crystal.

Step 5 (optional): Calculate the PPM accuracy budget

Finally, you can use the formula below to estimate the PPM accuracy budget for the whole application:

$$PPM_{Budget} = PPM_{crystal} + Deviation(C_L) \times Pullability_{crystal}$$

where:

PPM_{Budget} is the estimated accuracy for the oscillation frequency.

$PPM_{crystal}$ is the crystal PPM accuracy specified in the datasheet.

Deviation (C_L) is expressed in pF. It measures the deviation of the load capacitance (C_L) due to tolerances on load capacitor values and the variation of the stray capacitance (C_S) due to PCB manufacturing process deviation.

Pullabilty is expressed in PPM/pF (refer to *Section 3.7: Crystal pullability*).

Note: The PPM budget calculated above does not take into account the temperature variation which may make the PPM budget bigger.

5 Tips for improving oscillator stability

5.1 PCB design guidelines

The 32 kHz crystal oscillator is an ultra-low-power oscillator (transconductance of a few µA/V). The low oscillator transconductance affects the output dynamics since smaller transconductance values generates a smaller oscillating current. This results in a lower peak-to-peak voltage on the oscillator outputs (from a few dozen to a few hundred mV).

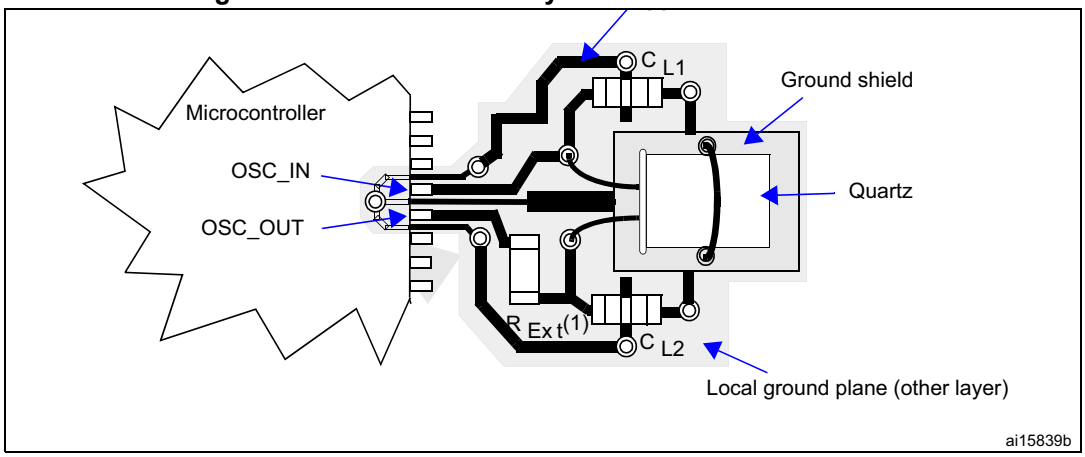
Keeping the signal-to-noise ratio (SNR) below acceptable limits for a perfect operation of the oscillator means more severe constraints on the oscillator PCB design in order to reduce its sensitivity to noise.

Therefore, great care must be taken when designing the PCB to reduce as much as possible the SNR. A non-exhaustive list of precautions that should be taken when designing the oscillator PCB is provided below:

- High values of stray capacitance and inductances should be avoided as they might lead to uncontrollable oscillation (e.g. the oscillator might resonate at overtones or harmonics frequencies). Reducing the stray capacitance also decreases startup time and improves oscillation frequency stability.
- To reduce high frequency noise propagation across the board, the microcontroller should have a stable power supply source to ensure noiseless crystal oscillations. This means that well-sized decoupling capacitor should be used for powering the microcontroller.
- The crystal should be mounted as close as possible to the microcontroller to keep short tracks and to reduce inductive and capacitive effects. A guard ring around these connections, connected to the ground, is essential to avoid capturing unwanted noise which might affect oscillation stability.

  Long tracks/paths might behave as antennas for a given frequency spectrum thus generating oscillation issues when passing EMI certification tests. Refer to *Figure 11: PCB with separated GND plane and guard ring around the oscillator* and *Figure 13: Signals around the oscillator*.
- Any path conveying high-frequency signals should be routed away from the oscillator paths and components. Refer to *Figure 11: PCB with separated GND plane and guard ring around the oscillator*.
- The oscillator PCB should be underlined with a dedicated underneath ground plane, distinct from the application PCB ground plane. The oscillator ground plane should be connected to the nearest microcontroller ground. It prevents interferences between the oscillator components and other application components (e.g. crosstalk between paths). Note that if a crystal in a metallic package is used, it should not been connected to the oscillator ground. Refer to *Figure 10: Recommended layout for an oscillator circuit*, *Figure 11: PCB with separated GND plane and guard ring around the oscillator* and *Figure 12: GND plane*.
- Leakage current might increase startup time and even prevent the oscillator startup. If the microcontroller is intended to operate in a severe environment (high moisture/humidity ratio) an external coating is recommended.

Figure 10. Recommended layout for an oscillator circuit



Warning: **It is highly recommended to apply conformal coatings to the PCB area shown in *Figure 10*, especially for the LSE quartz, CL1, CL2, and paths to the OSC_IN and OSC_OUT pads as a protection against moisture, dust, humidity, and temperature extremes that may lead to startup problems.**

5.2 PCB design examples

Example 1

Figure 11. PCB with separated GND plane and guard ring around the oscillator

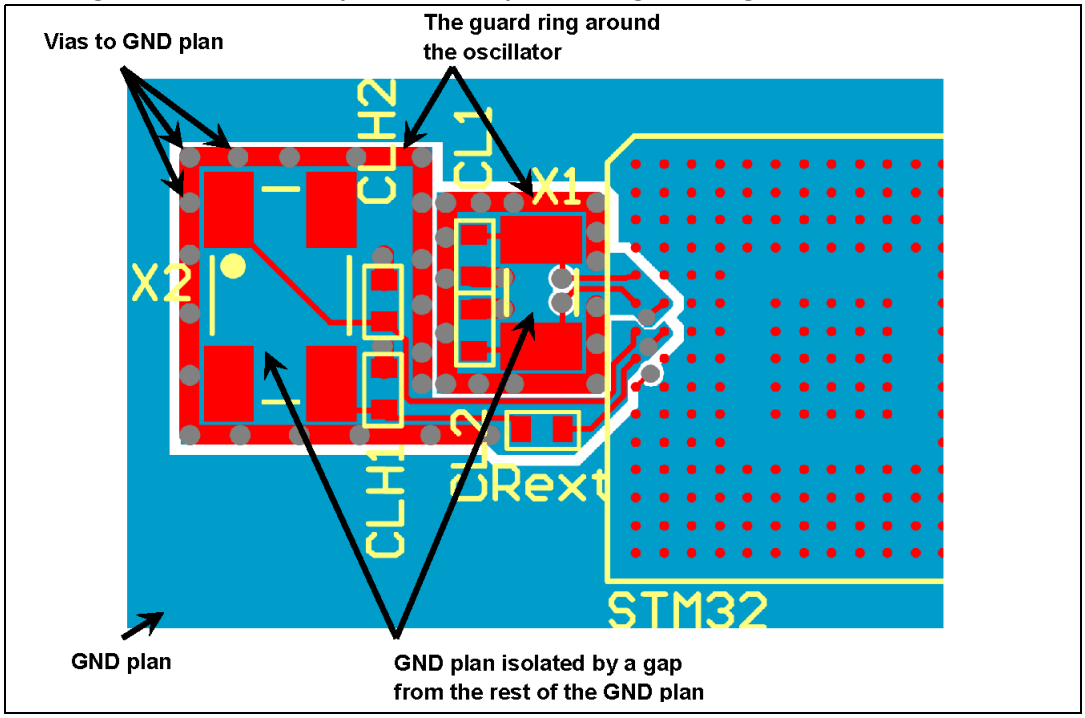


Figure 12. GND plane

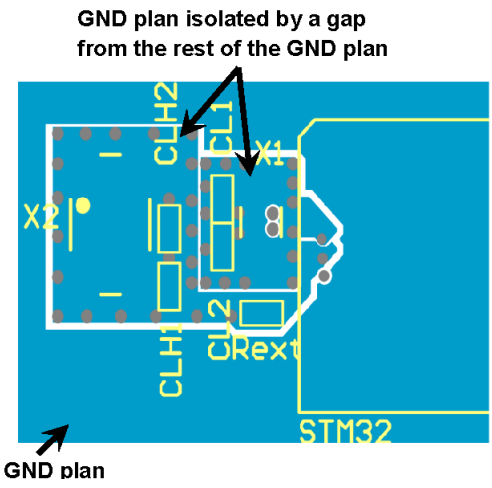
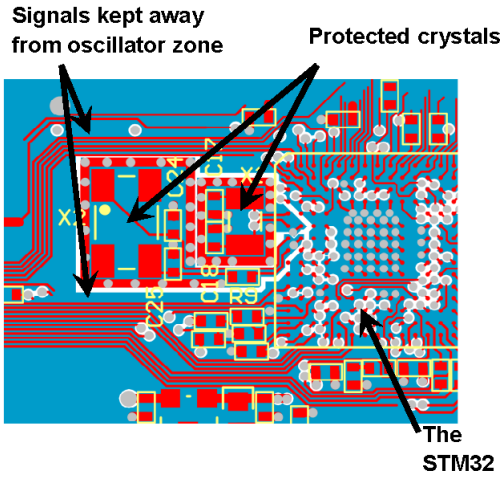


Figure 13. Signals around the oscillator

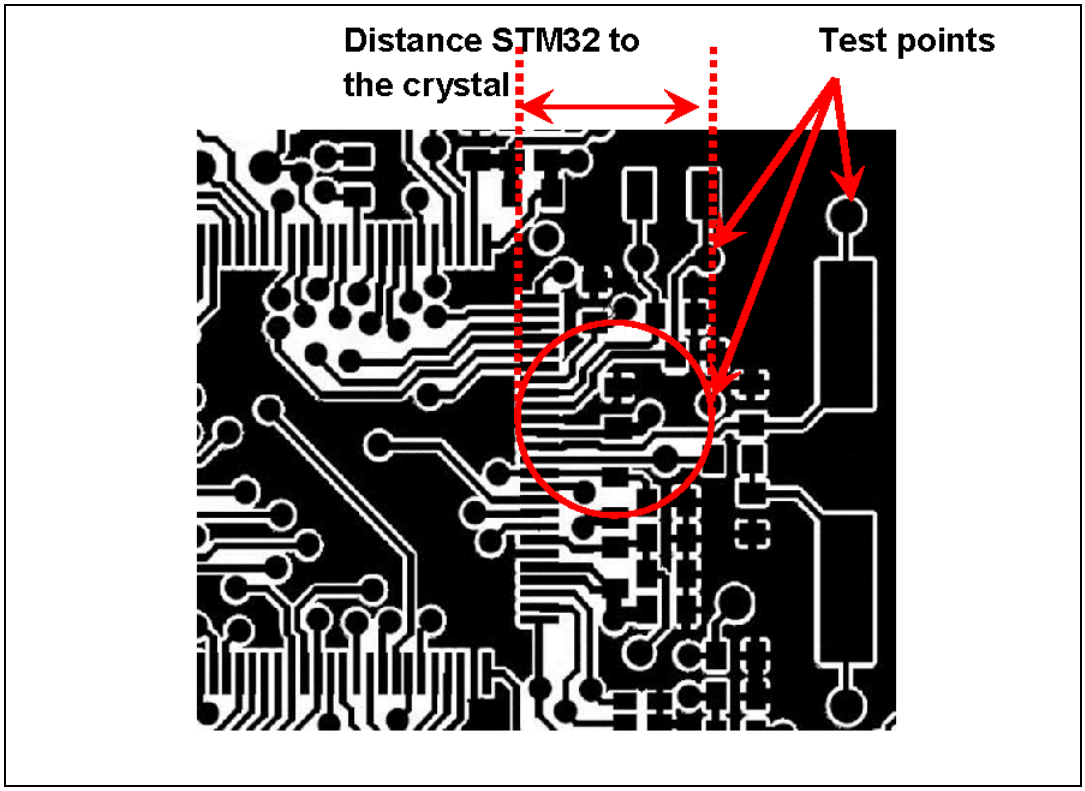


Example 2

Figure 14 gives an example of PCB that does not respect the guidelines provided in *Section 5.1*:

- No ground plans around the oscillator component
- Too long paths
- No symmetry between oscillator capacitances
- High crosstalk/coupling between paths
- Too many test points.

Figure 14. Preliminary design (PCB design guidelines not respected)



The PCB design has been improved to respect the guidelines (see *Figure 15*):

- Guard ring connected to the GND plane around the oscillator
- Symmetry between oscillator capacitances
- Less test points
- No coupling between paths.

Figure 15. Final design (all design guidelines have been respected)

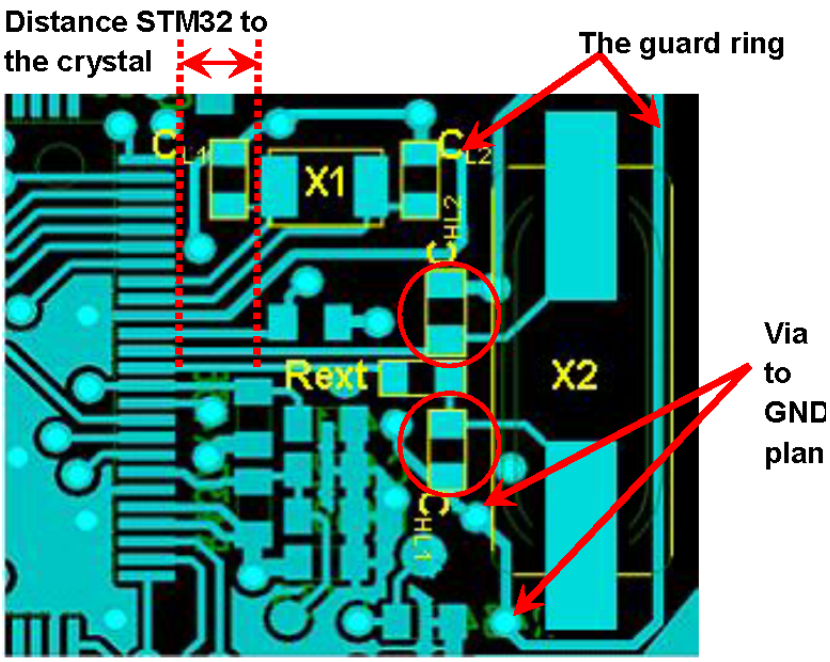


Figure 16. GND plane

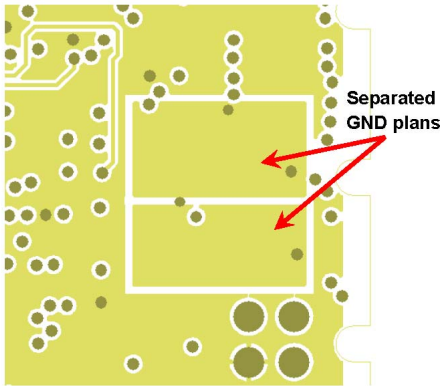
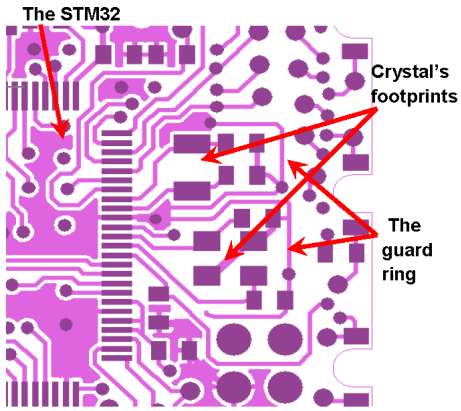


Figure 17. Top layer view

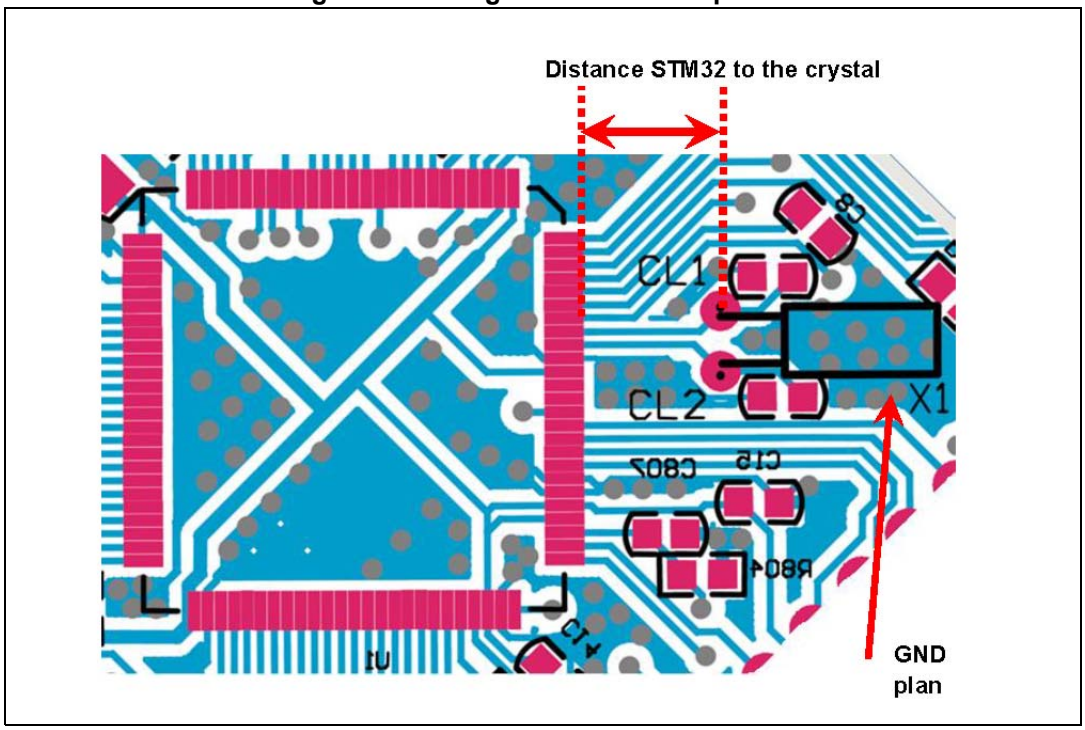


Example 3

Figure 18 gives another example of PCB that does not respect the guidelines provided in *Section 5.1*:

- No guard ring around oscillator components
- Long paths
- EMC tests failed.

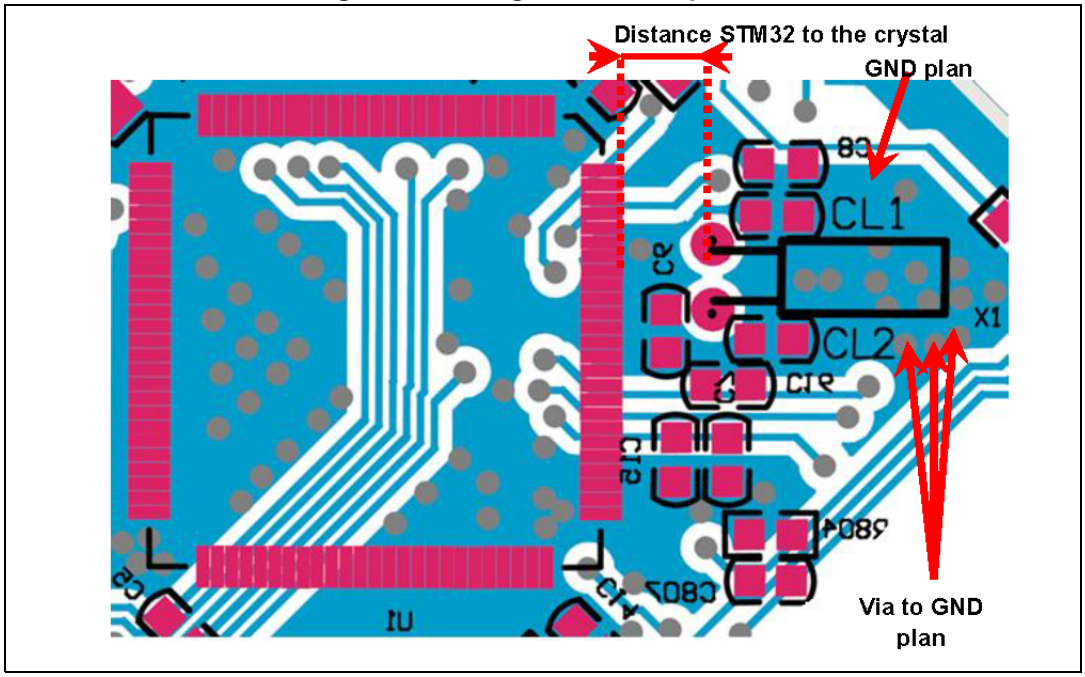
Figure 18. PCB guidelines not respected



The PCB design has been improved to respect the guidelines (see *Figure 19*):

- Ground planes around the oscillator component
- Short paths that link the STM32 to the oscillator
- Symmetry between oscillator capacitances
- EMC tests passed.

Figure 19. PCB guidelines respected



5.3 Soldering guidelines

In general, soldering is a very sensitive process for low-frequency crystals more than it is for high-frequency ones. Hints to reduce the impact of such process on the crystal parameters are provided below:

- Expose crystals to temperatures above their maximum ratings can damage the crystal and affect the ESR value. Refer to the crystal datasheet for the right reflow temperature curve. If it is not provided, ask the manufacturer.
- PCB cleaning is recommended to obtain the maximum performance by removing flux residuals from the board after assembly (even when using “no-clean” products in ultra-low-power applications).

6 Reference documents

- [1]
  E. Vittoz *High-Performance Crystal Oscillator Circuits: Theory and Application* IEEE Journal of solid State Circuits, Vol 23, No 3, June 1988 pp 774 - 783.

7 FAQs

Table 6. Frequently asked questions

Questions	Answers
How can I know if my crystal is compatible with a given STM32 MCU?	Refer to *Section 4: Guidelines for selecting suitable crystal and external components*.
In my application, 32.768 kHz frequency very-low drift and high accuracy are mandatory to obtain an accurate clock without calibration. Which crystal load capacitance (C_L) can I choose?	First, you should make sure that your crystal is compatible with the selected STM32 LSE. Then, it is highly recommended to use a crystal with low pullability, that is with $C_L \geq 6$ pF: $C_L = 7$ pF is a good compromise between low drift and moderate power consumption. 9 and 12.5 pF can be used in a noisy environment but will impact the power consumption.

8 Conclusion

The most important parameter is the gain margin of the oscillator, which determines if the oscillator will start up or not. This parameter has to be calculated at the beginning of the design phase to choose the suitable crystal for the application. The second parameter is the value of the external load capacitors that have to be selected in accordance with the C_L specification of the crystal (provided by the crystal manufacturer). This determines the frequency accuracy of the crystal. The third parameter is the value of the external resistor that is used to limit the drive level. In the 32 kHz oscillator part, however, it is not recommended to use an external resistor.

Because of the number of variables involved, in the experimentation phase you should use components that have exactly the same properties as those that will be used in production. Likewise, you should work with the same oscillator layout and in the same environment to avoid unexpected behavior and therefore save time.

Recently MEMS oscillators have emerged on the market with a significant market share. They are a good alternative to resonators-based oscillators thanks to their reduced power consumption, small size (they do not require additional passive components such as external load capacitors) and their competitive cost. This kind of oscillators are compatible with the whole STM32 microcontrollers except for STM32F1 and STM32L1. When a MEMS oscillator is paired with an STM32 embedded oscillator, this latter should be configured in bypass mode.