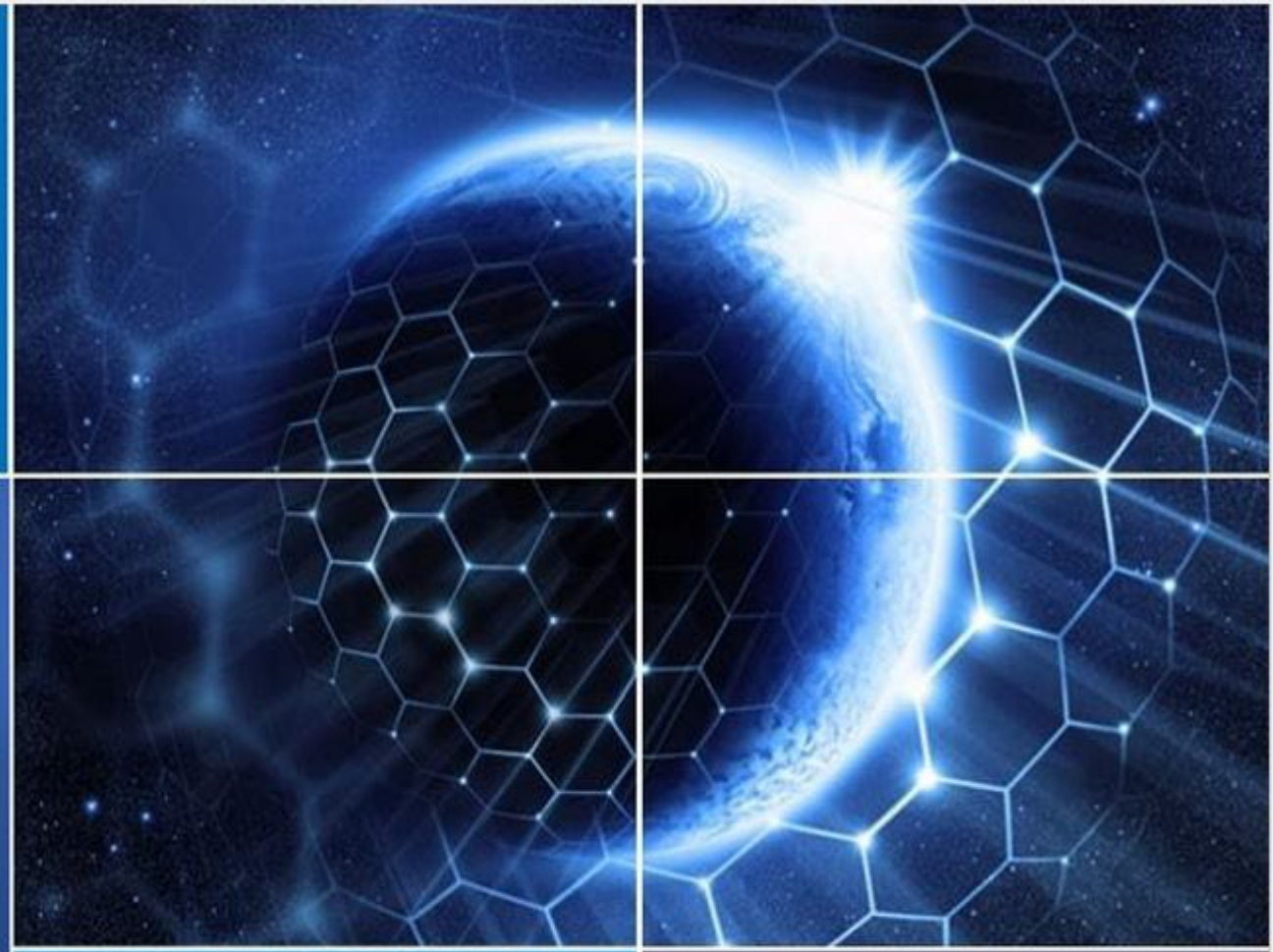
Oscillator Design Optimization

Negative Resistance and Oscillator Circuit Margin

Nov. 2022

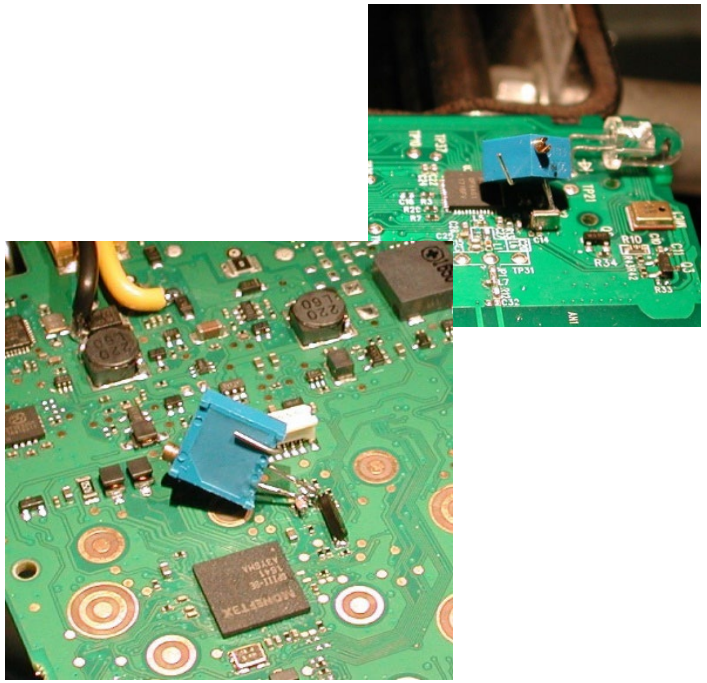


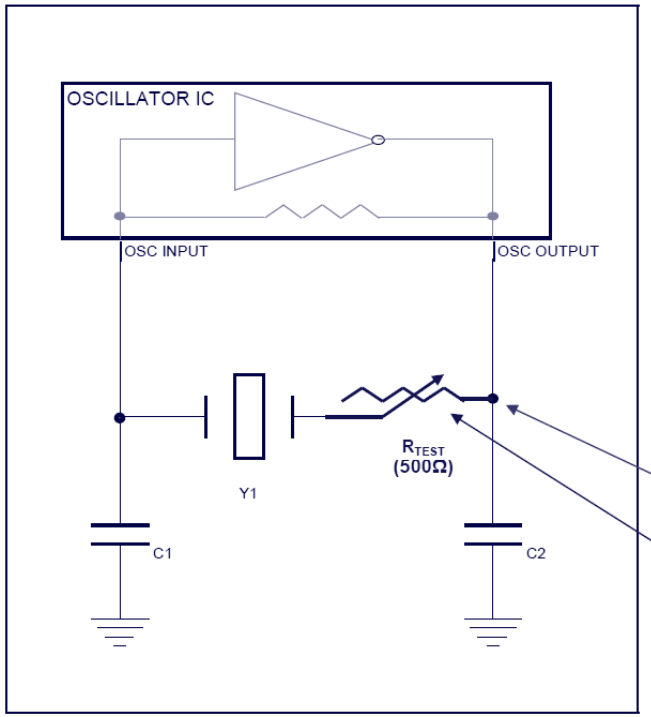
RALTRON

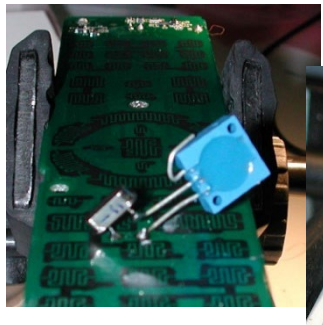
Negative Resistance and Oscillator Circuit Margin

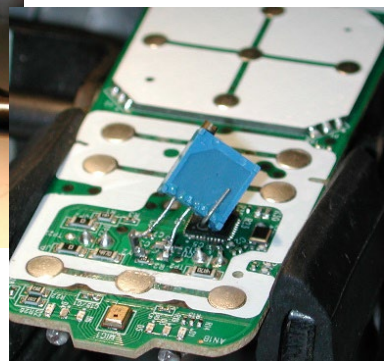
CIRCUIT MODIFICATION FOR DETERMINATION OF NEGATIVE RESISTANCE "NegR"

Negative Resistance/Circuit Margin is performed with a balance of good frequency match (least amount of measured frequency shift from a crystals measured accurately on a test system and then in circuit). The load capacitor values in circuit (C_1 and C_2) directly effect the amount of Negative Resistance and the Frequency, so this is balanced with the C_L (capacitive load) of the crystal for optimum performance.









TOUCH HERE WITH ACTIVE/FET PROBE ONLY FOR WAVE SHAPE

ADD A VARIABLE RESISTOR IN SERIES TO CRYSTAL

Negative Resistance and Circuit Margin Calculation

- To start the calculations a good known crystal is needed; if the ESR of the crystal is not known, the values for C_0 and C_L of the crystal unit must be known in order to determine ESR along with the R_1(RR) which is the measured Resistance at Frequency Resonance. **(Formula A)**

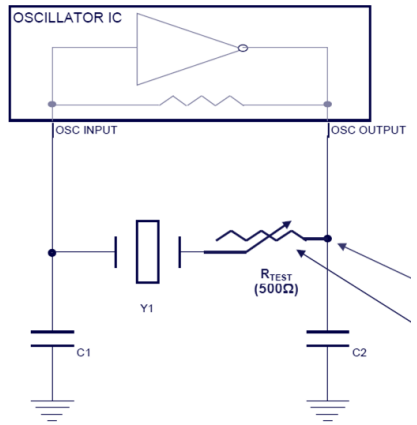
(A) Determine ESR of crystal unit:

$$ESR = R_1\left(1 + \frac{C_0}{C_L}\right)^2$$

R_1 = RR = Rs of crystal unit

C_0 = shunt capacitance of crystal unit

Refer to the later slides 5 for spec parameter C_L and slide 6 for the measured R_1/RR and C_0.



- In order to determine the negative resistance a variable resistor(10 to 20 turn potentiometers for better adjustment accuracy) is added in series to the crystal unit. A 500 Ω resistor is a good value to start with. but could go up to 10 kΩ for MHz crystals or 1 MΩ for kHz crystals using.

- Increase the resistance of the variable resistor until oscillation stops, slowly turn it back until the oscillation just starts up again. Stop at this point.

Negative Resistance and Circuit Margin Calculation

- Take the variable resistor 'R_{TEST}' out and measure the adjusted resistance using a resistance meter.

- Add the value of 'R_{TEST}' into the equation to determine **Negative Resistance** of the circuit and then calculate the **Circuit Margin (CM). (Formulas B and C)**

(B) Calculate Negative Resistance

$$NegR = R_{TEST} + ESR$$

R_{TEST} = Measured value of variable resistor

(C) Determine Circuit Margin

$$CM = \frac{NegR}{ESR_{AVG}}$$

ESR_{AVG} = Average ESR of typical crystal lot

(D) RESULT:

For an optimally designed circuit the 'Negative Resistance' would be better than 100 Ω; while the Circuit Margin would be greater than 10. A Circuit Margin between 5 to 10 would be acceptable. A Circuit Margin below 5 could have 'start-up' problems and failures in manufacturing and in the field may occur.

Crystal Spec Parameters

Example of MHz Crystal Parameters

	PARAMETER	VALUE
	NOMINAL FREQUENCY	54.000 MHz
	MODE OF OSCILLATION	Fundamental
	FREQUENCY TOLERANCE AT 25°C	±6 ppm max
	AGING	±1 ppm first year max
	TOTAL STABILITY	± 20 ppm max
C_L	LOAD CAPACITANCE	19 pF
ESR	EQUIVALENT SERIES RESISTANCE	15 Ω max
C_0	SHUNT CAPACITANCE	0.9 ± 25% pF
	PULLING SENSITIVITY, MAX	3.5 ppm/pF ± 15% (at C_L: 19 pF)
	DRIVE LEVEL	350 µW max

Example of kHz Crystal Parameters

	PARAMETER	VALUE
	NOMINAL FREQUENCY	32.768 kHz
	MODE OF OSCILLATION	Fundamental
	FREQUENCY TOLERANCE AT 25°C	±20 ppm max
	AGING	±3 ppm first year max
C_L	LOAD CAPACITANCE	7 pF
ESR	EQUIVALENT SERIES RESISTANCE	70 kΩ max
C_0	SHUNT CAPACITANCE	1.1 pF typ
	DRIVE LEVEL	0.5 µW max
	INSULATION RESISTANCE	500 MΩ min @ DC 100 V

Crystal Spec Parameters

Examples of Test Data:

To calculate the ESR.

*C_L per specification

*Measured RR (R_1)

*Measured C_0 (Shunt Capacitance)

Saunders 250B

Reference Fr: 32,000,000.00 (Using Measured FL)

Power: 100.00 µW Into RR

PL: 0.00 ohms C_L: 10.00 pF

Crystal	First Failure	RR Ω	C_0 pF	C_1 fF	C_L pF
High Limit		50.00	2.00		
Low Limit			0.00		
1	PASS	7.85	1.35	4.39	9.51
2	PASS	6.17	1.37	4.61	9.52
3	PASS	8.15	1.33	4.50	9.64

Reference Fr: 32,768.00 (Using Calculated FL)

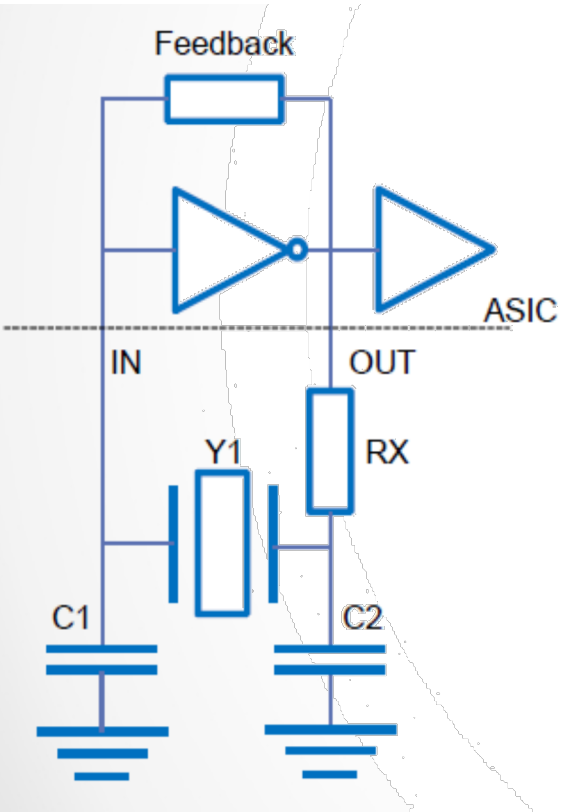
Power: 500.00 nW Into RR

PL: No Load C_L: 7.00 pF

Crystal	First Failure	RR kΩ	C_0 pF	C_1 fF	C_L pF
High Limit		70.00			
Low Limit		1.00			
1	PASS	46.34	1.46	6.45	6.80
2	PASS	35.21	1.27	4.93	7.20
3	PASS	35.45	1.26	4.92	7.20
4	PASS	36.69	1.27	4.87	7.20

Recommended Steps to Increase Negative Resistance and Improve Circuit Margin

If the Negative Resistance is too low and or the crystal ESR is too high, the Circuit Margin can be too low if less than 5.0. To increase the Negative Resistance/Circuit Margin:



1. Lower the value of Rx (current limiting resistor) to increase the crystal drive if this is an option.

2. Lower the values of C_1 and C_2 to increase Negative Resistance.
   a. A decrease in C_1 and C_2 capacitive value will increase the on-board frequency.
   b. Using a crystal plated to a lower C_L (Capacitive Load) will need smaller values of C_1 and C_2 for a good frequency match.

3. Use a crystal with a lower ESR. Lower ESR when divided into NegR will give a higher CM.

4. Where possible use a different IC with ALC (Automatic Level Control) which adjusts the drive level as needed to ensure there is enough drive and negative resistance to have a consistent crystal signal amplitude level.