RALTRON
A RAMI TECHNOLOGY Company

COMMON SENSE OSCILLATOR TECHNIQUES

INTRODUCTION.

ASICs and microprocessor clocking elements market size is estimated at 100 million units per month. Often these requirements were satisfied by designing mother-boards with thru-holes and the purchase of "full size" or "half size" logic clocks. Driven by PCMCIA and disk drive designers, updated oscillator cells are now included in most ASICs. These oscillator cells can be used to provide time base clock outputs without the necessity of a packaged clock. This technique permits PCB real estate reduction of 60% which in turn has the added advantage of reducing EMI. Clocking costs are reduced directly and additional cost reductions indirectly when one considers space costs.

It is the fundamental purpose of this paper to indicate to the novice ways to utilize the oscillator cells in ASICs to provide clocking requirements. This paper will discuss the effects of output impedance, the external components, and the methods for selecting same.

FUNDAMENTALS. Oscillators may be categorized as either of the relaxation or harmonic type. Relaxation oscillators consist of a single energy storage element (capacitor or inductor) and a resistor. The C-R or L-R time constant is usually used to trigger a device sensitive to a voltage level such as a flip-flop or a Uni-Junction Transistor (UJT). Waveforms are typically exponential in nature and rich in harmonics. The frequency of oscillation is determined by the time constant, supply voltage, and threshold trigger level. In general these oscillators are not very frequency stable but function well for strobes, turning indicators or flashing lights.

Harmonic oscillators conform to Barkhausen's criteria, requiring both phase and gain criteria be satisfied to provide sustained oscillator.

Σ Gain around a close loop ≥ 1

Σ Phase shifts around a closed loop = n * 360 deg where n is an integer value

Harmonic oscillators utilize both inductive and capacitive elements or their mechanical and sonic equivalents, such as the elements represented in the equivalent circuit of a quartz crystal. Harmonic oscillators are characterized by sinusoidal waveforms and excellent frequency stability. The frequency is determined by the inductors and capacitors and the propagation delay in the active circuitry. This paper will be limited to the generation of harmonic oscillations using the new oscillator cells.

10400 N.W. 19th Street • Miami, Florida 33172
Tel: 305-593-6033 • Fax: 305-594-3973

RELAXATION OSCILLATOR	HARMONIC OSCILLATOR
Flip-Flop	L/C (Inductor/ Capacitor)
Uni-Junction Transistor	Crystal
	Ceramic Resonator

CRYSTAL CHOICES. Oscillator design for clocking must be simple, low cost and reliable. The basic AT and BT cuts invented in 1934 [1] are still the cuts of choice. AT cuts are used in both fundamental and overtone modes. BT cuts are used in the fundamental mode only.

AT Cut. AT cut resonator's frequency vs. temperature characteristics follow 3rd order curvature with an inflection point at +25C. Standard frequency vs. temperature specifications are ±0.005% (50 ppm) or ±0.01% (100 ppm) from -20C to +70C. Stability limits are ±0.001% (10 ppm), from -20C to +70C.

BT Cut. BT cut resonator's frequency vs. temperature characteristics follow a parabolic curve with the maximum frequency near room temperature. Consequently, for the BT cut, the frequency decreases at both higher and lower temperatures. A crystal that is calibrated to nominal frequency at +25C will be -100 ppm at +70C and will be changing at -4 ppm per degree C.

See figure 1 for a graphical comparison of both cuts.

AT Fundamental Strip. Low cost miniature fundamental AT strip crystals are commonly used from 3.5 to 40 MHz. Crystal resonator design specified that the plate's thickness (in mils) = 66.4 / Frequency (in MHz). Strip crystals are troubled with flexure and face shear coupling that must be accounted for in the width to thickness design ratio. In addition, the upper and lower frequency limits are restricted by process design and difficulties. At the low end of the frequency spectrum, the thickness is almost 20 mils and requires special processing such as uni-directional contouring and edge tilting. At 40 MHz, the AT crystal is only 1.66 mils thick and must be handled with vacuum picks.

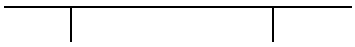
AT Third Overtone Strip. In designing overtone strip crystals, coupling problems restrict the upper frequency limits to about 55 MHz. In addition to having the flexure and face shear coupling modes common in fundamentals, there are also couplings to the harmonic of both Z thickness shear and X thickness shear modes. Dworksy[2] states, "Clearly overtone design of strip resonators is much more complicated than fundamental mode device design, and tighter tolerance requirements for repeatable device performance are to be expected."

BT Fundamental Strip. Low cost miniature fundamental BT strip crystal resonators are 1.521 times thicker than AT crystals. The thicker resonator reduces the cost of processing so it follows that many strip crystal units in the 30 to 45 MHz frequency band are fundamental BT plates.

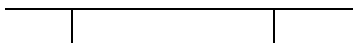
Inverted Mesa Crystals. Inverted Mesa crystals utilize and etching technique to manufacture bi-level resonators. The thicker, lapped portion is used for mounting support. The thinner, etched portion contains the electrode. Fundamental crystals are available from 60 to 120 MHz and third overtones to 350 MHz. A new product, tab mesa crystals, has recently been marketed. This product uses less than the full 360 degree thicker support region and can be packaged in 2- x 6-mm tubular packages.

HC-49 and HC-45 Fundamental and Third Overtone Crystals. Fundamental and 3rd overtone crystal housed in conventional HC-45 and HC-49 holders are also excellent choices as clocking elements. These crystals are leaded devices that should be thru-hole mounted. Third leads can be added for more rugged, low profile mounting. Lead forming for SMT applications can be done; however, due to processing and handling difficulties, this is presently not a big ticket item.

10 MHz 20 MHz 30 MHz 40 MHZ
Fundamental AT strip resonator



30 MHz 40 MHz
Fundamental BT strip resonators



40 MHz 50 MHz
3rd O.T. AT strip resonators.

Strip Crystal Ranges.

ASIC CELLS OSCILLATOR BASICS.

The most widely used oscillator today is the MOS gate oscillator using an unbuffered inverter. Almost all microprocessors, along with many other digital applications, have this circuit built inside the cell or are driven from an external oscillator using this ASIC circuit.

Oscillator cells have several characteristics that are important to the oscillator designer.

R_{in} R_{in} is high -10 Meg ohms

R_{out}. R_{out} is dependent on the type of logic being used. ECL logic has low impedance – in the range of 7 ohms. CMOS logic has higher output impedance – in the region of 700 ohms. HCMOS logic is typically between 250 and 500 ohms. An oscillator designer should obtain the output impedance information from the manufacturer. If this information is not available, a simple output impedance test circuit is described in figure 2.

Gain. Gain is derived by biasing an inverter in a linear mode. Biasing is done by connecting a resistor from the inverter's output to input. This connection results in high gain and wide bandwidth, but both lack consistency.

Phase shift. Phase shift at f_0, the frequency of oscillation is approximately 180 degrees through the amplifier from input to output. An additional 180 degrees phase is derived from the pi feedback network. To insure reliable start-up and stable operation, the

circuit must have the ability to shift phase an additional 20 degrees beyond the 180 degree minimum feedback requirement.

Phase shift is modified by the time delay from input to output of the amplifier – typically 1 to 2 nanoseconds. Since frequency is the reciprocal of time, time delay is equated to additional phase shift of the inverter. The external pi circuit must shift 180 degrees less than the delay's equated shift.

Table I shows phase shift for 1 and 2 nanosecond delay at selected frequencies. This reduced phase shift information will be useful in Bode plot analysis.

$$Phase\ lag\ (degrees) = \frac{time\ delay * 360}{period\ of\ f_0}$$

The designer should make sure there is sufficient dynamic range to make up for component or power supply change. For example, a finger in a circuit will disturb phase shift and allow a crystal to start, lock on, and continue to oscillate.

To meet Barkhausen's phase shift criteria, we must shift 180 degrees externally (plus a minimum of 25 additional degrees) in the feedback loop. To design a stable oscillator, it is desirable to have fast rate-of-change-of-phase at the 180 degree point. To get 180 degrees phase shift across the pi network, we need to phase shift 90 degrees on both ends of the crystal. On the ASIC input side of the crystal, the crystal current flowing into C_1 will shift 90 degrees if Z_{in} is high. On the ASIC output side of the crystal, phase shifting should be going through 90 degrees, less the effective phase shift from the inverter's time delay – reference Table 1.

Basic Feedback Circuit. A basic Pierce oscillator circuit is shown in Figure 3. Components include the phase shifting elements C_1 and C_2 and an output impedance adjusting resistor, R_x. Note R_x is a discrete circuit component and is not included in the output impedance of the inverter. If R_x is omitted in oscillator designs (and unfortunately many times it is), problems easily arise. The designer should always layout his circuit for this component and use a zero ohm resistor (short) if R_x is not required for his feedback configuration.

Feedback Element Selection. For this paper, feedback external to the ASIC cell will be reduced to a "pi" or parallel tank configuration. It is noteworthy that a "T" configuration has similar characteristics but is not within the scope of this paper. There are four (4) possible combinations of reactance's that can occur with a non-loaded tank-circuit. These four cases are shown in Figure 4.

Figure 4, case 1, has capacitors in both legs and a mutually connected inductor. The circuit will oscillate only if an inductor is placed in the Z_3 location. An example of Case 1 is the common Pierce configuration often used in crystal oscillator circuits. Connecting a crystal satisfies the oscillation condition slightly above Fs on each crystal mode. The circuit will capture the mode with the lowest real term. During most of

the frequency spectrum, the crystal is capacitive and no oscillation will occur. Reference figure 5 for reactance vs. frequency response of a crystal's resonator.

Both case 2 and 3 cannot oscillate if either a capacitor or inductor is externally connected.

Case 4 can oscillate if a capacitor is connected between the terminals. Connection of a crystal may not be productive since the crystal's reactance is capacitive over most of the frequency spectrum. Oscillation can occur at multiple frequencies since the crystal can satisfy the required impedance both below F_s and above F_a. One must be careful in this configuration.

Frequency (MHz)	Period - 360 deg (nsec)	1 nsec Equiv Phase Shift (deg)	2 nsec Equiv Phase Shift (deg)
10	100	3.6	7.2
25	40	9	18
50	20	18	36
75	13	27	54

Table I - Phase shift vs. gate delay for selected frequencies

Impedance Matching. Oscillator circuits depend on the rate-of-change-of-phase for stability. The importance of the rate-of-change-of-phase can be seen graphically when one considers a shift in frequency due to a perturbation, component change, moisture, act of God, etc. The oscillator will not satisfy Barkhausen's phase criteria at the old frequency so it changes phase until oscillation can occur. Suppose an unstable circuit shifts phase 2 degrees. This may cause a frequency changed 6 Hz or the phase slope is 1/3 deg/Hz. Typically, we desire a phase slope of 40 degrees per Hz. If an impedance match is made at the input and output of a pi network, the phase slope is lowered considerably. Consequently, the designer should strive for a large mismatch to maximize the phase slope. This all must be done with common sense in control.

As an example of impedance matching, consider inserting a capacitor into a 110 Volt wall socket and attempting to shift the Power Company's phase. Obviously, this doesn't work because the signal source has very, very low impedance. If a series resistor was inserted with a resistance equal to the reactance of the capacitor, the phase shift would be 45 degrees at the R-C junction and the signal amplitude would be reduced by ½.

This same phenomenon occurs on the output of the ASIC. If the output impedance is low compared to the external reactance, the capacitor will not significantly shift the

phase. Stated simpler, a small C_2 connected to the output of a low impedance ASIC does nothing. If R_x is added, (R_x = X_{C2}) 45 degree phase shifting will occur at the crystal. Probably the most important consideration in this paper is the choice of C_2 with respect to the output impedance of the ASIC cell. Reference Figure 6.

Observe that if R_x is a short, $R_{ou}t$ is directly in parallel with C_2. The Q of the output matching network is defined as $R_{ou}t + R_x$ divided by X_{C2}. Textbooks would like a Q of 10. Consider compromising and letting Q ≈ only 2. If the circuit above is operating at 40 MHz and the cell has an output impedance of 200 ohms, C_2 should be 39 pf – not unreasonable. If an ECL gate is used with a Q of 1, C_2 should be 560 pf – which is unreasonable.

Using the Thevenin equivalent of the output driver, one can recognize that the phase shift at the output – C_2 junction is very much a function the choice of C_2. Using the Norton equivalent, we observe that the output impedance is directly across C_2.

Bottom Line. If the Q is less than 2, increase Rx or increase C_2 – within limits. Accept Q = 2 minimum. Design for Q = 5 minimum.

ASIC Drive Capability. The drive capability of the ASIC cell must be considered in selecting components. The capacitor current (i) = dQ/dt, therefore Q = ∫i*dt. The voltage is then the integral of i*dt/C. The output driver must be able to charge C2 in a short period of time. If C2 is small, it can quickly be charged; however, if C2 is larger and the ASIC output driver has limited gm, the capacitor will not charge significantly and the voltage developed on C2 will be very limited.

The output signal from the cell not only drives C2 externally, but is also the same signal driving the next internal logic elements used to produce the system's clock signal. If this signal is small in amplitude, it should be cause for concern. Logic levels should switch from 20% to 80% of VDD at the output of the ASIC.

If small signal is observed at the output of the ASIC*, there are two methods of increasing signal level – reduce the load (capacitance) of C2 or increase the value of Rx. ** If Rx's value is chosen to equal XC2, the signal amplitude at the crystal will be ½ the signal going to the system clock. The addition of Rx will reduce crystal drive level, reduce EMI and increase phase shifting resulting in a higher reliability, more stable system.

* Measure signal only with a non-loading FET probe such as Tektronix Model P6204. Measuring with a common 8 to 12 pf passive probe is not allowed.

** Increasing the value of Rx will increase the output signal level until a point where crystal losses cannot be made up. At this point, the signal level will start to decrease. Recall Art Laffer's curve on taxation revenue vs. tax rate?

Bottom Line: Design for large signal on the ASIC output – 4 Volts p-p for 5 Volt logic. Measure signal only with a FET probe.

Voltage Gain From the Output to Input. The voltage level feeding back from output to input through the passive elements may be smaller or larger than the signal at the output. At first glance, it may sound strange that signal can be increased through passive elements; however, if the gate input has high resistance, it can be shown that the output signal is charging a tap on a tank circuit and the passive voltage gain is approximately equal to C_2/C_1.

$$\frac{Vin}{Vout}\ (Voltage\ Gain) = \frac{C_2}{C_1}$$

To verify the passive gain phenomena, place a non-loading scope probe on the input of the cell (same as on C_1). Remove C_1. Observe the signal increases until the ESD diodes limit the signal.

Bottom line: To make up signal losses through the crystal, choose:

$$C_2 = 1.1 * C_1\ to\ 1.5 * C_1 \text{ (3)}$$

Feedback Resistor. The feedback resistor is used to bias the input of the inverter in a class A configuration. The size of the resistor should be large enough to prevent loading of the feedback network and allow the inverter to operate in the center of its range.
For fundamental modes and overtone oscillators with tank circuits, R_1 should be 0.5 to 1.0 Meg ohms at high frequencies and from 1 to 5 Meg ohms at lower frequencies.

For inductorless 3rd overtone, the selection is more critical and will be only a few thousand ohms.

SPECIFYING CRYSTAL.

Series or Parallel ? Parallel !

Resistance. Low crystal resistance is desirable for better stability and higher reliability. Low resistance crystals are also inversely proportional to cost.

For parallel resonate crystals, the resistance should be specified as Effective Series Resistance (ESR).

$$ESR = R_M * (1 + \frac{C_0}{C_L})^2$$

Where R_m is the motional resistance, C_0 is the static capacitance and C_L is the load resistance.

Bottom Line: Resistance should be specified as low as practical, and practically may include economic factors.

Load Capacitance. For parallel resonate crystals, the load capacitance must be specified – assuming you know the load. This is not a "Which came first – the pothole or the wheel?" scenario. The oscillator design should specify what type of components should be purchased. The crystals on order or in stock should not dictate oscillator design.

Although more detail of C_L selection is covered in the next section, crystals are generally specified from 12 to 20 pf C_L for this type of application.

OSCILLATOR DESIGN DETAILS.

Caveat. The following element values are suggested starting values that may need iterations and require testing.

Testing. Testing should be performed on a breadboard that simulates the final product. Application of starting voltage should include both a slow ramp-up and a step function (this may require removal of the PCB supply voltage and apply VDD from an external variable power supply).

During power supply slow ramp testing of overtones, one may expect that operation will be on the fundamental until the supply reaches about 2.5 Volts. Corrections for lower mode starting are often done by decreasing the capacitance value of C2.

Power supply step function testing of both fundamental and overtone designs require instantaneous application of power. This may be done by lifting the ASIC VDD lead and touching it to VDD. This testing should include all voltages up to the ASIC's absolute maximum – usually 7.0 Volts. During step function testing at high voltage, the oscillator may try jumping to the next higher mode. This is not an acceptable condition. Corrections usually include increasing the value of C_2.

Load Capacitance. Load capacitance is specified as the capacitance placed in parallel with a crystal's leads that will cause the oscillator to operate at f_0. PCB stray capacitance and ASIC input/output capacitance contribute to the load. C_1 and C_2 are in series with each other. Calculation of C_1 & C_2 require that the stray capacitance must be added to all calculations. A typical configuration has approximately 10 pf stray capacitance on both the input and output.

For a first draft, calculate load capacitance without any accommodations for stray, input, or output capacitance. If the design calculations for C_1 & C_2 specify 10 pf C_L, use a 15 pf crystal.

C_1 and C_2 will be calculated using the 5 pf assumption.

To solve for C_L: $C_L = \frac{C_1 * C_2}{C_1 + C_2}$

To solve for C_1: $C_1 = \frac{C_L * C_2}{C_2 - C_L}$

Common Circuit Choices. Figure 7 shows 6 common designs used for ASIC crystal oscillator operations.

The first circuit (A) is used for fundamentals – both AT and BT cuts.

Circuit (B) is the preferred choice for overtones.

Circuit (C) (D) and (E) are occasionally used – but not recommended by this author.

Circuit (F) is an alternate for (B) at highest overtone frequencies if (B)'s driver is limited.

Fundamental Mode Design. The operation of fundamental mode oscillator show in circuit (A) has been well documented (4), (5), and (6). Suggested values are shown in Table II.

The inductorless method can be understood by observing the effect of shunting the crystal with a low value resistance. A parallel resonate circuit of a capacitor, inductor and resistor has a reactance vs. resistance plot as shown in figure 8. Notice that the maximum inductance this circuit can generate is at the -3 dB point and has a value of

$$X_L\ Max = \frac{Q * X}{2}$$

The Q of a parallel resonate circuit is defined as the parallel resistance divided by either reactance:

$$Q = R/X_L$$

Rearranging above: X_L Max = R/2.

In figure 9, the parallel tank circuit's inductor is replaced with the inductance of a crystal. A plot is generated for 2 values of shunt resistance. We observe that we can shrink the diameter of the circle and therefore the maximum attainable value of inductance.

To suppress the fundamental mode and operate on the 3rd, the shunt resistor (R1) must be lowered. Figure 10 illustrates use of a 2,000 ohm shunt resistor across the crystal with a 5 pf load capacitor. Note that the vector "B" is –j3000 ohms at 10 MHz. The crystal's reactance cannot supply the +j3000 ohms (the limit is $R_1/2$) as shown by vector "A" which is the same amplitude and opposite phase as vector "B". Oscillation on the fundamental will not occur.

For the 3rd overtone, the same 5 pf load now has –j1000 ohms as shown by vector "D". Vector "C" is of the opposite phase and same amplitude. Now Barkhausen's phase criteria has been satisfied and the oscillator can only operate at f0 = 30 MHz.

The load's capacitance reactance will decrease by 1/3 at the third overtone; the amount of inductive reactance required there also decreases by 1/3. If Barkhausen's phase criteria requires a given inductive reactance from the crystal to operate in the fundamental mode, and the proper value resistor is placed in parallel with the crystal, it will reduce the amount of inductive reactance below the desired value established by the load capacitance.

Overtone with Series Trap. The overtone oscillator with series trap is a Pierce configuration.

The fundamental trap is an additional series L/C circuit located in either the input or output of the cell. The series resonate components are calculated from the basic equation:

$$F_{fund} = \frac{1}{2 * \pi * \sqrt{L * C}}$$

Choice of trap location is optional. If located at the input of the cell, the Q will be high – effectively the Q of the inductor. If the trap is located on the output of the cell, the Q will be low – effectively output impedance of the cell + R_x divided by the reactance of the inductor. Locating the trap on the output will also tend to clean up the signal before it enters the crystal.

Turning the trap is very critical if the trap is in the cell input. Inductors typically are ±10% values. To be sure the trap is properly tuned, the capacitor should be adjustable. To be sure the trap stays tuned over temperature, the capacitor should have a negative temperature coefficient equal to that of the inductor. A small resistor may be added in series with the inductor to lower the Q to 20 and eliminate these problems.

The term "Effective Capacitance" is now applicable for the input or output leg with the series trap. Note that above resonance, a series trap becomes inductive and is in parallel with C_1. The voltage gain is now $C_{2,eff}$ / C_1 for the trap at the output or $C_2/C_{1,eff}$ for a trap across the input leg.

The cell output has standard R_x phase shifting resistor.

The C_2 follows output impedance rules

$$X_{C2,eff} \leq R_{out} + R_x$$

$$C_{1,eff} = 0.5 * C_{2,eff} \ to \ 1.0 * C_{2,eff}$$

Table IV and V are suggested values.

Overtone with Parallel Tank. The overtone oscillator with a parallel tank is also a Pierce configuration. The cell output has a standard R_x optional phase shifting resistor.

The reactance must be calculated using the effective capacitance in the tank leg.

$$X_{C2,eff} \leq R_{out} + R_x$$

$$C_{1,eff} = 0.5 * C_{2,eff} \ to \ 1.0 * C_{2,eff}$$

The parallel anti-resonate circuit may be located in either the input or output of the cell. The better choice for location is usually to output (it's best to filter unwanted modes before the crystal). The parallel resonate circuit should be tuned from 25% to 50% of the frequency distance between the fundamental and the third overtone. If tuned closer to the fundamental frequency, the circuit will have more effective capacitance at the third overtone frequency. If tuned closer to the halfway distance, the circuit will have higher gain and start easier. The parallel resonate components are calculated from the basic equation

$$F_{tune} = \frac{1}{2 * \pi * \sqrt{L * C}}$$

Table IV and V are suggested values.

Note: This circuit is also acceptable in many 5th overtone designs.

BODE PLOT ANALYSIS. Analysis of selected feedback circuits was performed using Micro-Cap Circuit Analysis Program. Figures 11, 12, and 13 are plots of the Inductorless Overtone (Figure 7, Circuit B) at 50 MHz. Figure 14 is the same crystal in Circuit F. Figures 15 and 16 are Circuit F at 30 MHz.

Figure 11 show the response for values in Table III, with a 25 ohm crystal at 50 MHz. For an inverter with 1 nsec delay, the phase shift required is 180 – 18 or 162 degrees. The signal losses are approximately 4 dB.

Figure 12 shows the results of changing R_x to 150 ohms. Note the rate-of-change-of-phase is steeper at the 162 degree region, the phase continues for an additional 10 degrees; however, the losses are an additional 2 dB.

Figure 13 shows a correction for figure 12 with the reduction of C_1 to 5 pf. R_x is still 150 ohms. This plot is very similar to the original Figure 11. Except for crystal load calculations, R_x and C_1 are a trade at 50 MHz.

Figure 14 is the same crystal in Circuit F with the values of Table VII. Note the circuit has faster rate-of-change because the feedback resistor has been increased.

Figure 15 shows the response of a 40 ohm, 30 MHz crystal in circuit F. Component values are per Table VII except R_x is a short. The point of operation will be close to the 180 degree point; however, the rate-of-change-of-phase is not very steep. Signal loss is minimal.

Figure 16 has 300 ohm Rx installed and C_1 is reduced to 10 pf. Note the signal loss is approximately the same; however, the phase shifting is faster at the 180 degree point. R_x and C_1 swap raised the gain and increased rate-of-change-of-phase.

SUMMARY. For fundamental applications, choose circuit "A". For overtones, choose "B" or "F". Layout all circuits for R_x. Design for large signal on the ASIC output. Use R_x to reduce signal on the crystal and prevent loading of the ASIC output. Keep $C_{2,net}$ larger than $C_{1,net}$ to make up for crystal losses. Test results.

Presented at the 16th Piezoelectric Devices Conference
sponsored by IEEE Ultrasonics, Ferroelectrics, and Frequency
Control Society on September 27, 1994, by Marvin Veeser

10400 N.W. 19th Street • Miami, Florida 33172
Tel: 305-593-6033 • Fax: 305-594-3973

REFERENCES

1. R.A Heising, “Quartz Crystals for Electrical Circuits” May 1947

2. L.N Dworsky, “AT Quartz Strip Resonators” Proc. 41 st Ann. Symp on Freq. Control, 1987.

3. VS500 Digital ASIC Data Book, Design Guidelines and Application Notes, NCR

4. “Micropower Crystal-Controlled Oscillator Design Using GE/RCA CMOS Inverters” RCA Application Note ICAN-8743, May 1987.

5. S.S. Eaton, “Timekeeping Advances Through COS/CMOS Technology” RCA Application Note ICAN -6086.

6. Tom Williamson, “Oscillators for Microcontrollers,” Intel Corporation Application Note AP-155, 1988

7. V. Bottom “The Theory and Design of Quartz Crystal Units” 1974.

Freq. (MHz)	ASIC W/ LOW R-OUT (200 ohms)				ASIC W/ HIGH R-OUT (600 ohms)			
	C_1	C_2	R_x	C_L	C_1	C_2	R_x	C_L
10	22	33	680	18	22	33	270	18
20	22	27	330	18	22	27	SHORT	18
30	15	18	270	15	15	18	SHORT	15

Table II - ASIC Pierce Values for Fundamental Mode Operation

Freq. (MHz)	C_1	C_2	R_F	R_x	C_L
30	12	17	4700	47	12
40	12	17	3300	27	12
50	10	10	2700	10	12

Table III - Inductorless 3rd Overtone Values for Rout = 250 ohms

Freq. (MHz)	C_3	L_1 (µH)	C_1	$C_{1,eff}$	C_2	R_x	C_L
30	75	3.3	27	22	27	82	18
40	75	1.8	22	17	22	47	15
50	75	1.2	22	17	22	27	15

Table IV - Overtone Component Values with Input Series Trap for Rout = 250 ohms

Freq. (MHz)	C_1	C_2	$C_{2,eff}$	R_x	L_1 (µH)	C_3	C_L
30	18	39	34	82	3.3	75	18
40	15	33	28	47	1.8	75	15
50	12	27	22	27	1.2	75	15

Table V - Overtone Component Values with Output Series Trap for Rout = 250 ohms

Freq. (MHz)	L_1 (µH)	C_1	$C_{1,eff}$	C_2	R_x	C_L
30	3.3	33	25	39	47	20
40	2.7	22	17	33	27	20
50	1.5	22	15	27	27	20

Table VI - Overtone Component Values with Input Parallel Shunt for Rout = 200 ohms

Freq. (MHz)	C_1	C_2	L_1 (µH)	C_{eff}	R_x	C_L
30	18	33	2.7	25	150	15
40	15	27	2.2	19	68	15
50	15	27	1.2	18	18	15

Table VII - Overtone Component Values with Output Parallel Shunt for Rout = 200 ohms

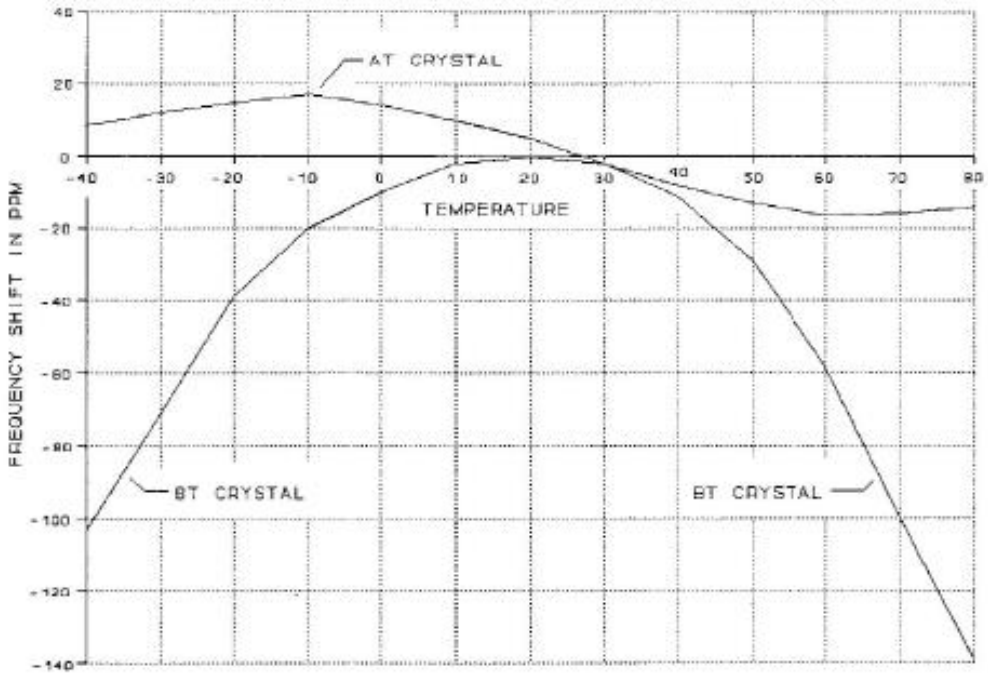
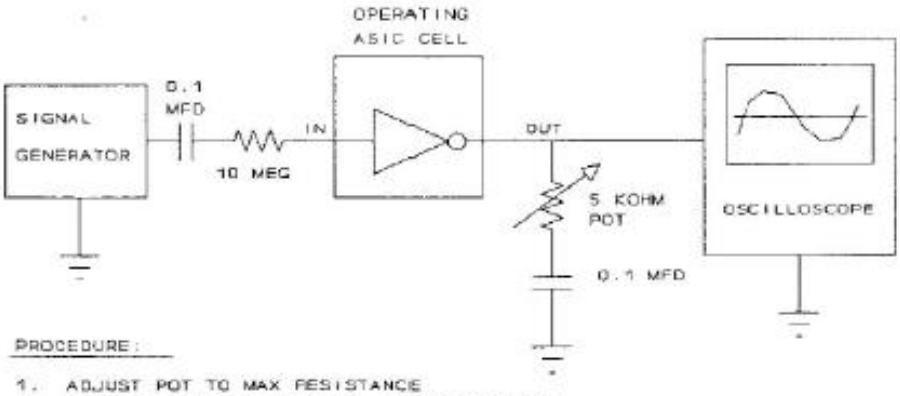


Figure 1 - AT and BT Curves Superimposed.



PROCEDURE:

1. ADJUST POT TO MAX RESISTANCE
2. ADJUST SIGNAL GENERATOR FREQUENCY TO Fo
3. ADJUST SIGNAL GENERATOR AMPLITUDE FOR APPROX 4 V P-P SINEWAVE ON SCOPE.
4. ADJUST POT TO REDUCE SIGNAL ON SCOPE TO 1/2 AMPLITUDE
5. REMOVE AND MEASURE POT WITH OHMMETER
6. POT RESISTANCE WILL BE APPROX EQUAL TO ASIC CELL OUTPUT IMPEDANCE.

Figure 2 - Rout Test Fixture.

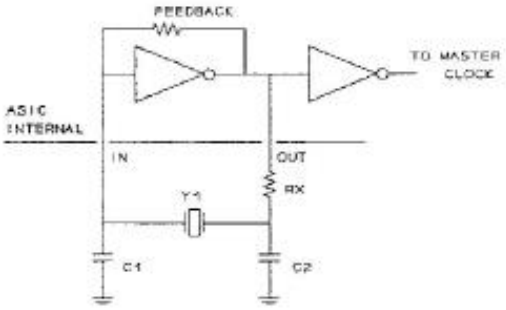


Figure 3 - Pi configuration.

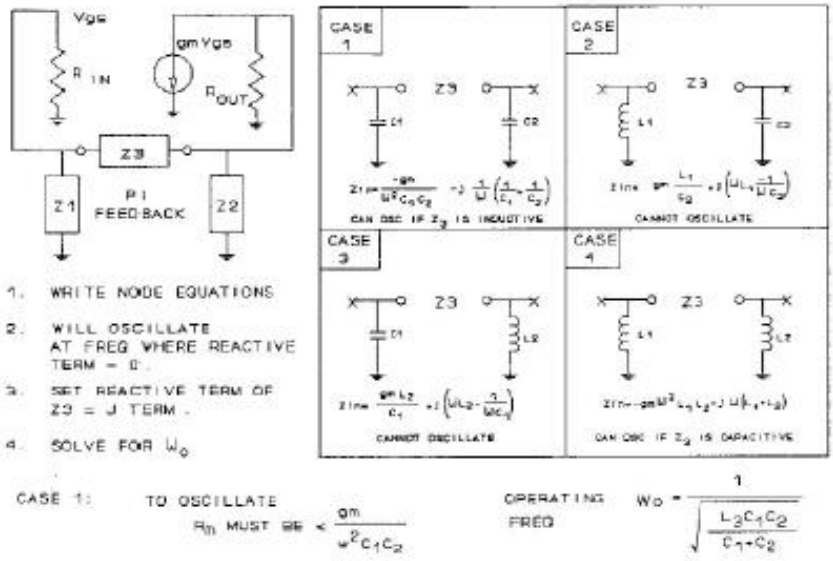


Figure 4 - Possible Configurations if Z3 is a Single Element.

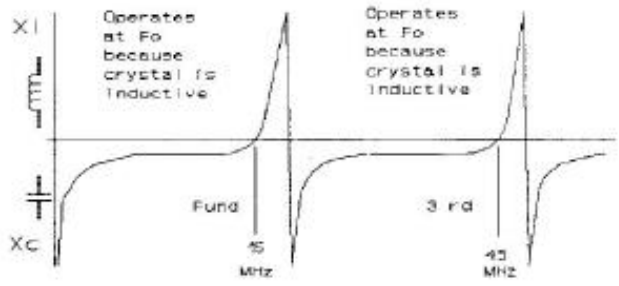


Figure 5 - Crystal Response.

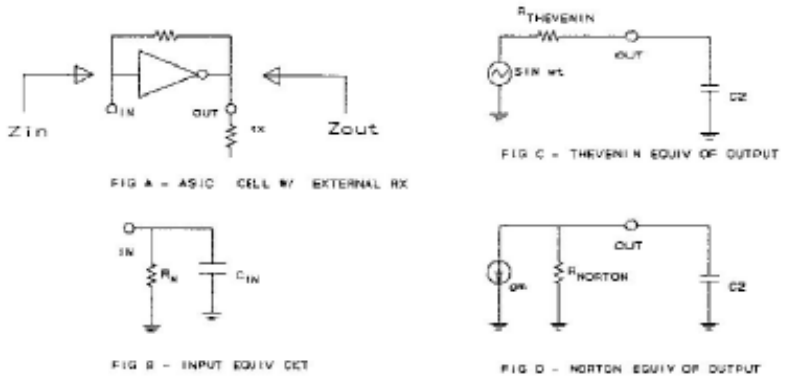


Figure 6 - ASIC Cell Input & Output Loading.

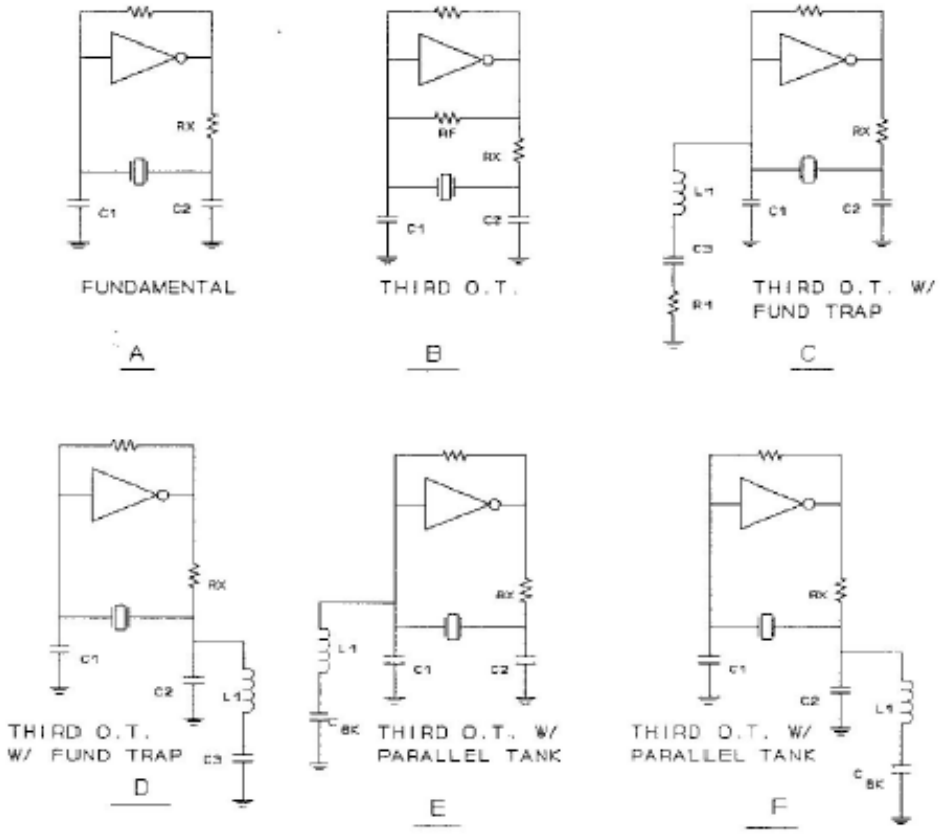


Figure 7 - Common ASIC Oscillator Configurations.

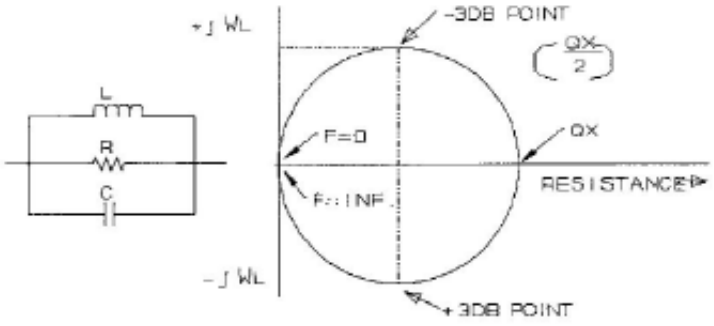


Figure 8 - Reactance vs Frequency for Parallel Resonate Circuit.

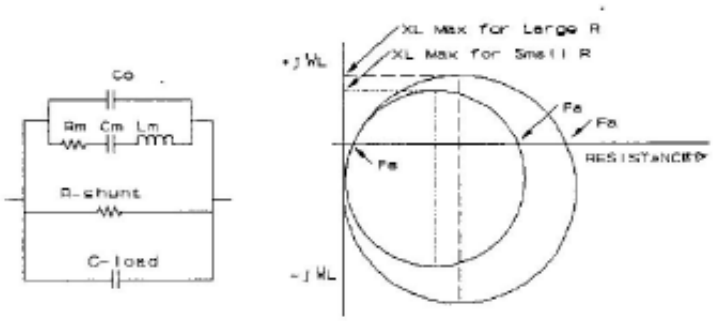


Figure 9 - Reactance vs Frequency for Crystal Shunted with Capacitance and Resistance.

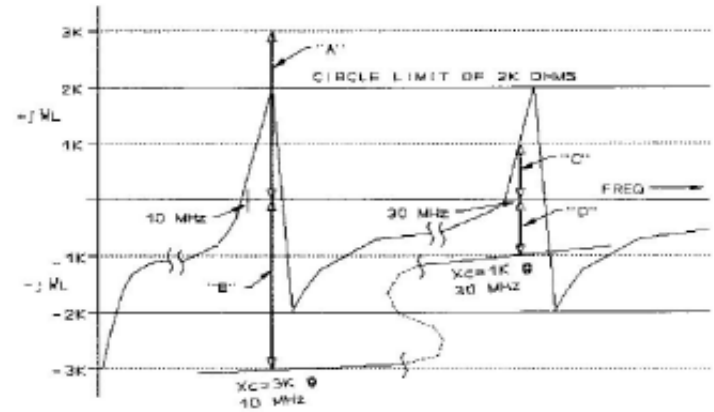


Figure 10 - Limiting Effects of Shunting Resistor in Oscillator Circuit.

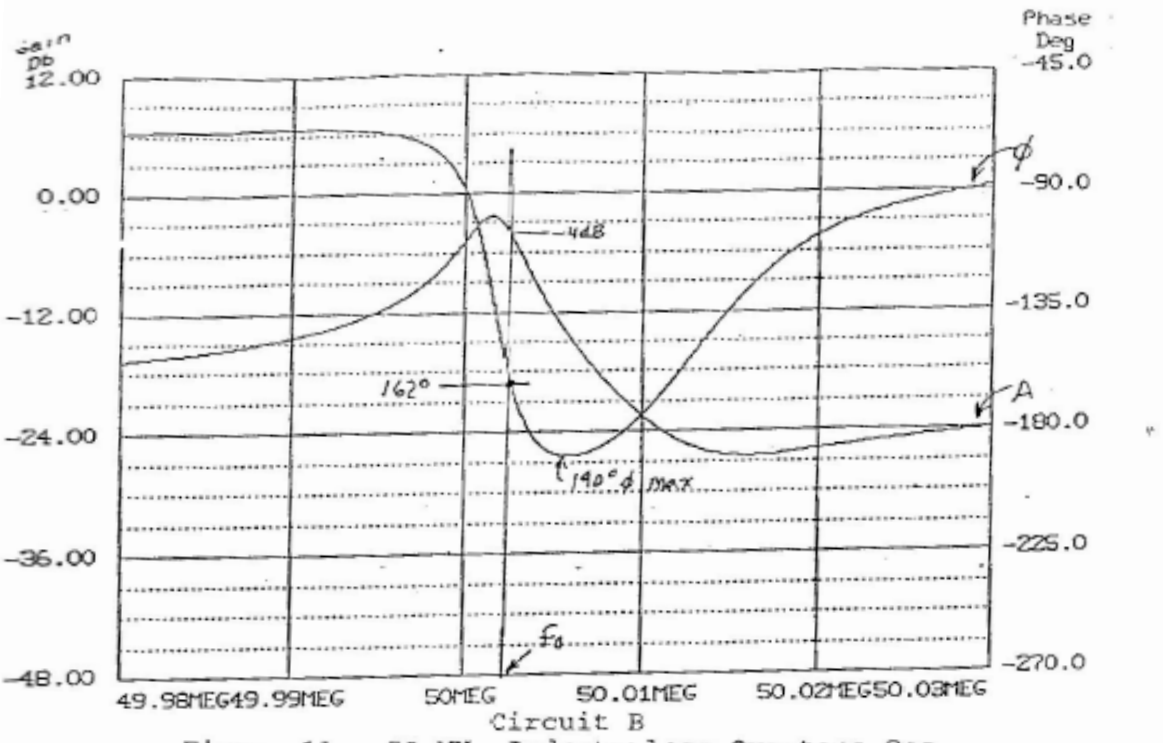


Figure 11 - 50 MHz Inductorless Overtone Osc.

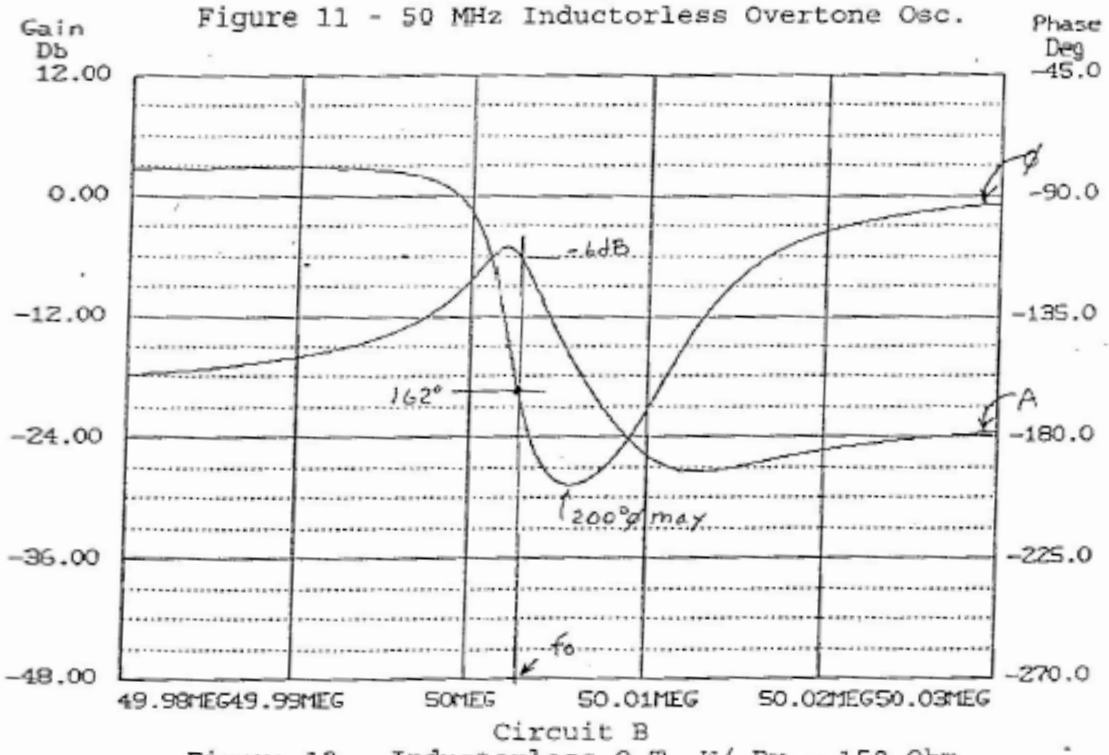
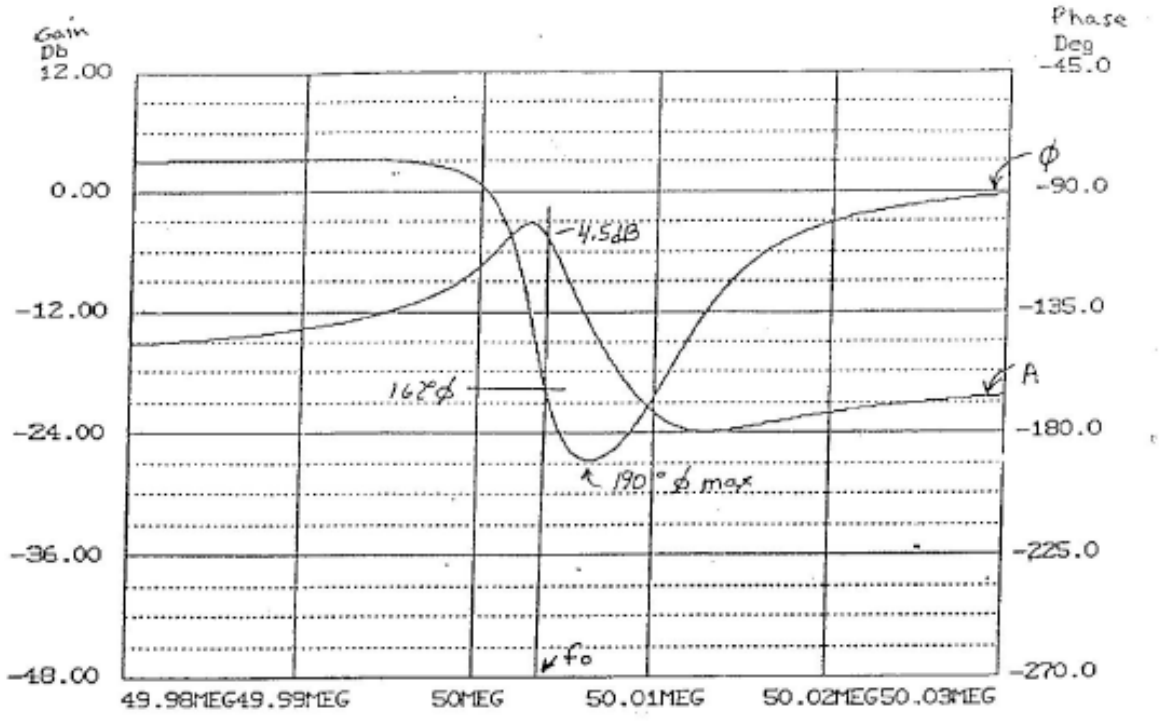


Figure 12 - Inductorless O.T. W/ Rx = 150 Ohm



Circuit B

igure 13 - Inductorless 3rd O.T. W/ Cin Reduced 5 pf & Rx = 150 ohm

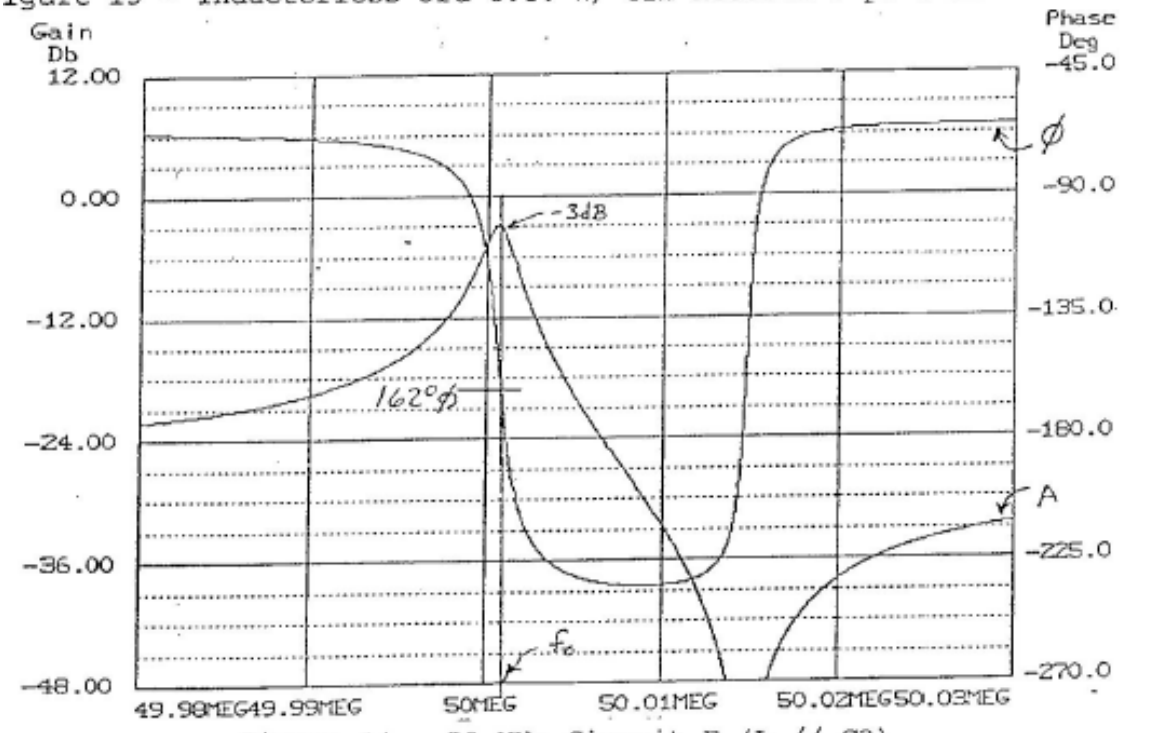


Figure 14 - 50 MHz Circuit F (L // C2)

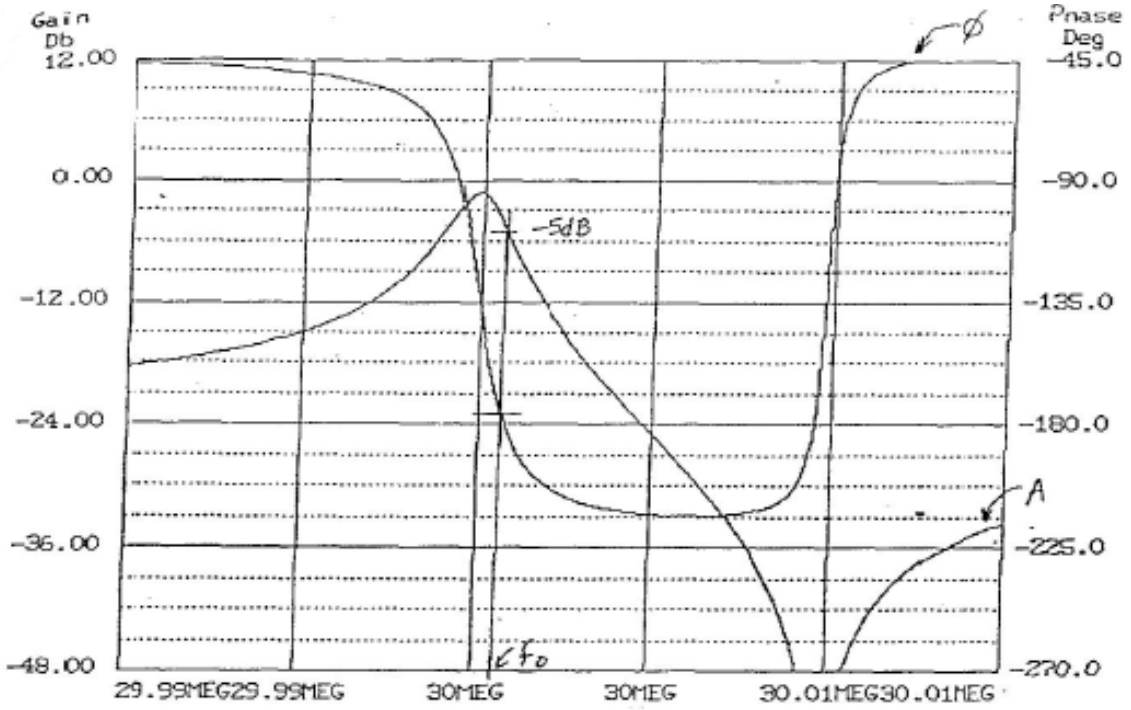


Figure 15 - Circuit F, 30 MHz w/ Rx = Short

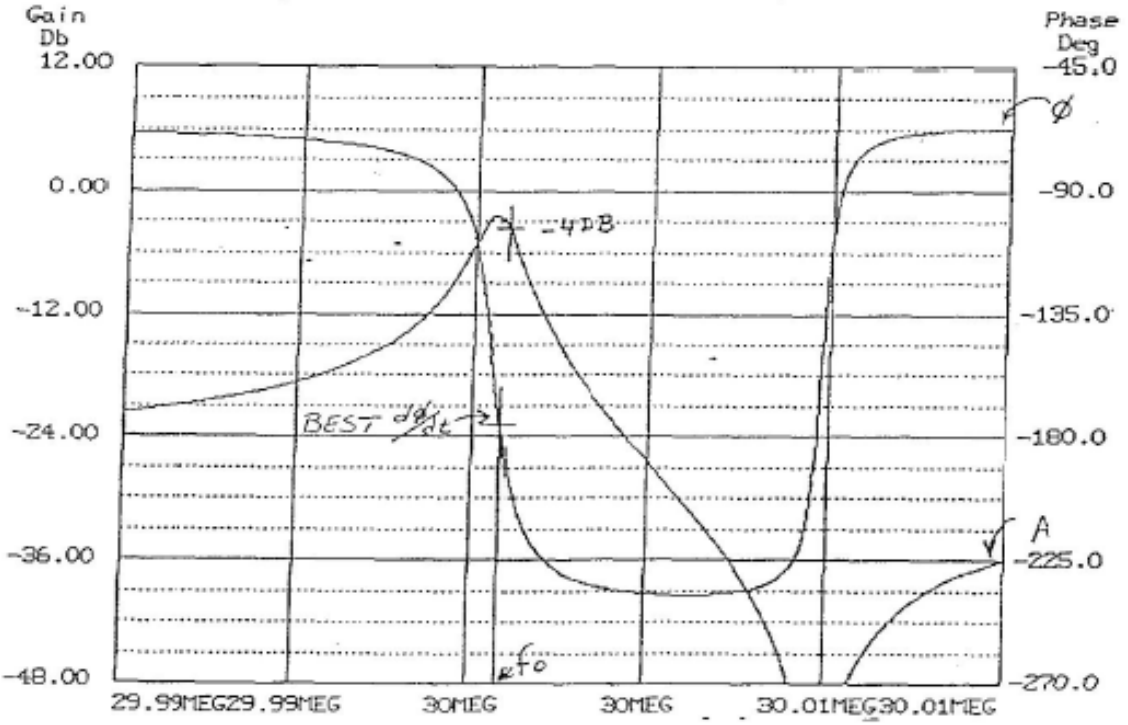


Figure 16 - 30 MHz Circuit F w/ Rx=300 ohm, C1 = 10pf