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COMMON SENSE OSCILLATOR TECHNIQUES,

THE SEQUEL

INTRODUCTION

Oscillator cells in ASICS have had a devastating effect on the sales of clock oscillators. Users have had the cost of clocking reduced at least 50%. Real estate reduction is often a factor of 10. In many user applications, the oscillator is one of only a few analog circuits remaining on the board rich in digital circuits. It is often the task of an engineer skilled in digital technology to design the analog circuit – often with the help of the ASIC manufacturer's Application Notes.

The App Notes from ASIC vendors often are written by gleaning a circuit that worked elsewhere at another frequency, driven by a different device. This combination of designers often leads to technical support calls to crystal manufacturers, usually after the PCB has been designed and into production.

Many large users tally failures of crystals in Defective Parts per Million (DPPM). After board assembly is done with high speed automatic assembly equipment, IR solder reflow techniques and automatic electrical testing, users are unhappy with 100 DPPM results.

Passive component levels of 15 DPPM are expected – often without the option of changing the sometimes less than optimum oscillator design.

It is the fundamental purpose of this paper to indicate to the novice some methods of improving the circuit designed around the ASIC cell. This paper will discuss the effects of limited gain, improved selection of external components, and methods for selecting same. This paper also includes a Lotus 1-2-3 spreadsheet program to calculate many of the parameters.

FUNDAMENTALS OF OSCILLATION

Harmonic oscillators must conform to Barkhausen's criteria, requiring both phase and gain criteria be satisfied to provide sustained oscillation.

Criteria #1: The summation of the gains around a closed loop shall be equal or greater than 1.

Criteria #2: The summation of the phase shifts around a closed loop shall be equal to N * 360 degrees phase, where N is an integer value of 0, 1, 2, etc.

Negative Resistance.

Negative resistance is a synonym for the gain of the amplifier. Several crystal suppliers' catalogs have similar, basic methods of measuring negative resistance.

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becomes 5 to 10 times larger than equivalent series resistance (CI value) of the quartz crystal unit.

CITIZEN: The negative resistance, also referred to as the degree of oscillation allowance, is one measure that can be used for judging the quality of the circuit-side oscillation motivity.

Method of Checking Oscillation Allowance of Oscillator Circuit.

1. *In order to confirm whether ample oscillation has been provided for the oscillator circuit or not, it is necessary to know the negative resistance (-R) of the oscillator circuit.*

2. *Insert… a variable resistor (VR) (for checking) in series with the quartz crystal unit. Then keep dropping the resistance until oscillation initiates. (In this case, disregard the drop in the oscillation output, and merely confirm oscillation.)*

   The negative resistance (-R) of this circuit, is the value obtained by adding the equivalent resistance of the quartz crystal unit to that of the variable resistor (VR) (used for checking).

3. *To assure the provision of an ample oscillation allowance for the oscillator circuit, adjust C_1, C_2, and R_d?? so that the resistance of the variable resistor (used for checking)*

EPSON: How to check the allowance for oscillation

1. *Connect the resistance (R) to the circuit in series with the quartz crystal.*

2. *Adjust R so that oscillation can start (or stop).*

3. *Measure R when oscillation just starts (or stops) in above (2).*

4. *Get the negative resistance – R=R+C_i value*

5. *Recommend –R |-R| > CI*(5 to 10)*

The above catalogs also have the following caveats.

Citizen: "The use of a circuit with an insufficient negative resistance may lead to such an unexpected trouble as the quartz crystal unit failing to initiate oscillation even when power has been switched on. "

EPSON: "Unless adequate negative resistance is allocated in the oscillation circuit, startup time of oscillation may be increased, or no oscillation may occur".

A third and more sophisticated method described in a paper given several years ago by Smith, Newell, Wordelman, Kenny

and Hartman titled *Oscillator Analysis Using S-Parameter Techniques*. This paper describes how a network analyzer with an S-Parameter test set can be used for measurement of negative resistance.

Negative resistance (-R) is the product of transconductance (gm) * XC1 * XC2. –R is reduced by a positive resistance such as output resistance, phase shift resistor, etc.

ASIC CELL CHARACTERISTICS.

Most of today's ASIC cells use a single stage unbuffered HCMOS inverter. The cells have high input impedance – typically 10 Meg ohms in parallel with 7 pf capacitance. The output impedance is much lower –100 to 500 ohms and has an effective output capacitance of 25 pf. Feedback capacitance from ASIC output to ASIC input is about 7 pf.

Negative resistance (-r) and delay time (td) through the ASIC is not standardized. The PCB often includes significant ground shielding to reduce EMI. This shielding and variable circuit trace length decreases the stability of the circuit and increases stray capacitance to a typical net of 7 to 10 pf.

IMPEDANCE MATCHING.

The choice of external components should consider desirability of impedance matching of the feedback circuit to the amplifier circuit. The tradeoff is frequency stability vs. power transfer. For maximum frequency stability in circuits such as TCXOs and OCXOs, mismatching is desirable. High stability circuits should be designed for large mismatches; that is, reactance's should be shunted with large resistive impedances. Mismatching will give high rate of change of phase at the operating frequency which is directly related to stability.

Logic clocks are not precise frequency references. Logic clocks require robust circuit designs. Desirable characteristics include fast start times, low EMI, no signal dropouts and abilities to overcome changes in circuit parameters such as small activity changes vs. temperature, external influences such as unremoved flux that may have collected conductive dirt or sometimes just a finger in or near the circuit. Logic clocks need the ability to transfer significant current through the crystal and therefore require closer matching of amplifier output impedance.

ASIC OUTPUT LOADING ON EXTERNAL CIRCUIT.

Previously it was mentioned that the output impedance of the typical ASIC is low. This impedance is directly in parallel with the capacitor C_2 – Reference Figure 1. This detail is one of the most overlooked errors in designing clock oscillators.

The Q of a capacitor is defined as $R_{parallel}$ / X_c. If C2 is selected with a reactance of –j500 ohms and the ASIC gate output impedance is 100 ohms, the capacitor will have a Q of 0.2 only. This is the equivalent of inserting a 2,500 ohm resistor in series

with C2. A low resistance in parallel with a small capacitor is a low resistance with no capacitance.

The minimum acceptable Q should be 2. If the Q is less than 2, increase Rx or increase C_2 – within limits. In the electrical testing evaluation, the waveshape entering R_x should be rail-to-rail squarewave. Exiting R_x, the signal should be a sinewave, 60% of VDD, peak-to-peak.

COMPONENT SELECTION AND CALCULATION

To assist in calculating the component values, a spreadsheet program has been written in Lotus 1-2-3. A program listing of the first two designs are included. A complimentary disk with the complete program is available from the author. Table I is a layout of the program. Use of the program can be simplified by referencing the program to Cell A1 (Home Key). Once referenced, either Page Down (or Page Up) and Tab (or Shift Tab) can be used to relocate for different configurations. The program does not calculate complex numbers.

Oscillator Circuit.

The basic Pierce oscillator circuits shown in Figure 1 are the first two circuits evaluated in the program and are the recommended choices for ASICs. Four other combinations of overtone circuits are included; however, only the last design is recommended for 5th and 7th overtone crystals.

Use of the program is simple. One needs to enter two resistance values, the ASIC or gate output resistance and the phase shift resistor R_x, two stray capacitance estimates and enter C_1, C_2, the Frequency and the Overtone Mode (when specified). Evaluate and iterate. Warnings are built to caution if voltage gain is too low, Q is too low or tanks are tuned beyond safe regions.

R_x is a discrete circuit component. The designer should always lay out his circuit for this component, and use a zero ohm resistor (short) if R_x is not required for his present configuration.

A parallel circuit may be located in either the input or output of the ASIC cell. The better choice for location is usually the output. It's best to filter unwanted modes before the crystal and keeping the low Q inductor off the input helps shifts phase. The parallel resonate circuit should be tuned from 25% to 60% of the frequency distance between the fundamental and the third overtone. If tuned closer to the fundamental frequency, the circuit will have more effective capacitance at the third overtone frequency. If tuned closer to the overtone, the circuit will have higher gain and start easier.

The overtone oscillator with series trap in either the input or output is a troublesome circuit. Since the trap must be tuned exactly at the fundamental frequency, select components should be required. If an inductor of a specific value is chosen and the inductor values move ±10%, the fundamental will lose attenuation of greater than 9 dB. Considering most low cost

inductors are ±20%, the trap can cause serious problems causing the oscillator to run on the fundamental or it may activate both modes simultaneously.

CRYSTAL UNIT CHOICES.

Crystal unit packages for microprocessor applications may be categorized in packages as either surface mounted devices (SMD) or leaded devices. SMD types almost always use strip crystals. Leaded units use strip crystals in the cylindrical package or HC-49S and circular crystals in the low cost HC-49 package. Typical choices and parameters are:

Crystal Load Capacitance.

Load capacitance is specified as the capacitance placed in parallel with a crystal's leads that will cause the oscillator to operate at f_0. PCB stray capacitance and ASIC input/output capacitance contribute to the load. C_1 and C_2 are in series and are calculated as product over sum. The spreadsheet program calculates crystal load capacitance two ways – using stray capacitance or using practical value of 7 pf total stray capacitance. Select crystal load capacitance from 16 to 20 pf (parallel) load. Do NOT use series crystals with ASICs.

Series resistance (RS) should be as low as practical. Reference 1 gives a good explanation of resistance/cost tradeoff. Effective Series Resistance (ESR) is a calculation that includes load capacitance and static capacitance. With strip crystals, C_0 is usually small and ESR is usually close to RS; however, if C_L is small and C_0 significant, the "effective" resistance may be much larger than R_S and could cause operation problems. Example: A crystal with C_0 = 7 pf and C_L = 16 pf will have ESR greater than twice R_S.

$$ESR = R_S * \left(1 + {C_0}/{C_L}\right)^2 \qquad (1)$$

Testing.

Testing should be performed on a breadboard that simulates the final product. Application of starting voltage should include both a slow ramp-up and a step function to verify that the design will always operate on correct mode at VDD ±20%. Testing for operating conditions is best checked at the output of the following stage. For signal level testing, use a Field Effect Transistor (FET) probe only. Standard probes with 8 to 12 pf loading are not allowed.

Testing of crystal current can be accomplished with an inexpensive current probe such as Tektronix CT-1. Power levels must not exceed rated levels.

CONCLUSION

The use of crystals in today's technology requires careful design by today's digital engineers. The slide rule can be replaced with the spreadsheet. Monitoring a few parameters can greatly improve the

reliability of product going into high volume production.

REFERENCES

1. Tom Williamson, “Oscillators for Microcontrollers,” Intel Corporation Application Note AP-155, 1988.

2. VS500 Digital ASIC Data Book, Design Guidelines and Application Notes, NCR

3. Warren Smith, D.E. Newell, James Wordelman, Dave Kenny, Kenneth Hartman “Oscillator Analysis Using S-Parameter Techniques”

4. M.A. Veeser “Common Sense Oscillator Techniques” 19th Crystal Conference, 1994.

5. “The CrystalMaster ‘93”, Product Catalog, Epson America, Inc.

6. “Quartz Crystal Catalog”, Citizen Watch Co. , Ltd.

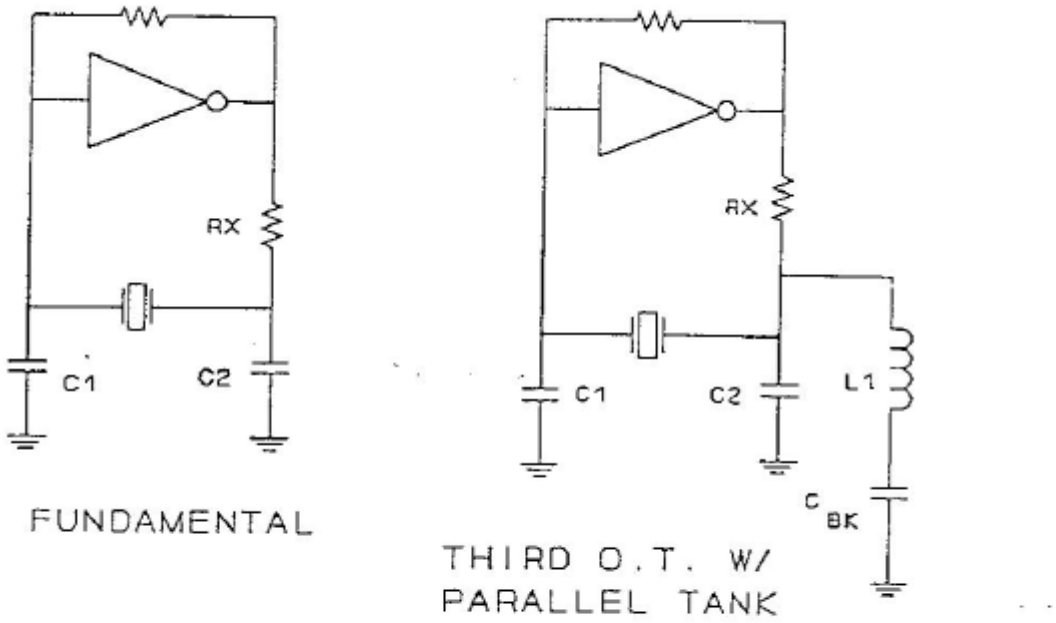

Figure 1
Common ASIC Fundamental and 3rd Overtone Circuits

User Instructions	User Instructions	Table of Resonate L-C Combinations
Calculations for Series Ckt.	Schematic for Series Ckt.	Table of X_c vs. Freq.
Calculations of O.T. Ckt. with parallel tank on ASIC output	Schematic of O.T. Ckt. with parallel tank on ASIC output	Table of X_1 vs. Freq.
Calculations of O.T. Ckt. with parallel tank on ASIC input	Schematic of O.T. Ckt. with parallel tank on ASIC input	
Calculations of 3rd O.T. Ckt. with series trap on ASIC output	Schematic of 3rd O.T. Ckt. with series trap on ASIC output	
Calculations of 3rd O.T. Ckt. with series trap on ASIC input	Schematic of 3rd O.T. Ckt. with series trap on ASIC input.	
Calculations of series trap and parallel tank Ckt.	Schematic of series trap and parallel tank Ckt.	

Table I - Lotus 1-2-3 Oscillator Component Evaluation

Pkg.	Cut	Mode	Min Freq. (MHz)	Max Freq.	Tol., -20/70 C
SMT or HC-49S	AT	Fund.	3.5	40	±0.005%
	AT	3rd O.T.	30	70	±0.005%
	BT	Fund.	35	45	±0.010%
Leaded HC/49-U	AT	Fund.	1	30	±0.005%
	AT	3rd O.T.	25	70	±0.005%

LOTUS 1-2-3 USER INSTRUCTIONS

This program is applicable for ASIC oscillator component selection. Program will calculate impedances for either parallel tank or series trap on either input or output of inverter. Circuit Q will be checked. Voltage gain form output to input will be calculated. Crystal load will be calculated using a practical method and an exact method, based on stray capacitance. Tables of resonate frequency and reactances can be accessed by entering Home, Tab, Tab, followed with PageDown.

Use PageDown for applicable program, Tab for applicable schematic.

Line 21 Fundamental Mode. Capacitance on ASIC output and input.

Line 41 3rd or 5th Overtone. Cap on ASIC input. Parallel tank on ASIC output.

Line 61 3rd or 5th Overtone. Parallel tank on ASIC input. Cap on ASIC output.

Line 81 3rd Overtone. Cap on ASIC input. Series strap on ASIC output.

Line 101 3rd Overtone. Series trap on ASIC input. Cap on ASIC output.

Line 121 5th and 7th Overtone. Combinations of both parallel tank and series traps on the output of ASIC.

FOR BEST RESULTS:

Use C_1 and C_2 reactances from 75 to 200 ohms. Observe net capacitances from input and output above green line on screen. Set voltage gain from ASIC output to ASIC input slightly above 1.

Estimate ASIC output impedance. Set Q on output circuit = 2 minimum. Use R_x and C_2 to adjust Q.

For parallel tank, tune tank from 25% to 65% distance between lower mode and operating mode. When set to 25%, tank will have maximum effective cap. When set to 65%, circuit will start faster.

CIRCUIT FOR FUNDAMENTAL MODE

Enter Frequency, stray C_{in} & Stray C_{out}, and GATE OUTPUT RESISTANCE. Iterate C_1, C_2 and Phase shift resistor (if available). VOLTAGE GAIN is NET C_{-OUT}/NET C_{-IN}. Should be slightly above 1. PRACTICAL and CALCULATED LOAD are crystal load capacitance.

FREQ 30.0 MHZ

GATE INPUT CIRCUIT	
C1	22 PF
STRAY CIN	8 PF
XC1	-241.1 OHMS, w/j
XC-STRAY C1	-663.1 OHMS, w/j
NET XC	-177 OHMS, w/j
NET C-IN	30.0 PF
VOLTAGE GAIN	1.2

GATE OUTPUT CIRCUIT	
C2	27 PF
STRAY C2	10 PF
GATE OUTPUT RES	150 OHMS
PHASE SHIFT RES	50 OHMS
XC2	-196.5 OHMS, w/j
XC-STRAY C2	-530.5 OHMS, w/j
NET X OF ALL C//L	-143 OHMS, w/j
Q	1.4
NET C-OUT	37.0 PF
XTAL LOAD, PRACT.	19 PF
XTAL LOAD, CALC.	17 PF

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CIRCUIT FOR PARALLEL TANK AT ASIC OUTPUT.

FREQ	40.0 MHZ
MODE	3 RD

------ GATE INPUT CIRCUIT --------

C1	22 PF
STRAY CIN	8 PF
XC1	-180.9 OHMS, w/j
XC-STRAY C1	-497.4 OHMS, w/j
NET XC	-133 OHMS, w/j
NET C-IN	30 PF
VOLTAGE GAIN	1.1
XTAL LOAD, PRACT.	18 PF
XTAL LOAD, CALC.	16 PF

------- GATE OUTPUT CIRCUIT --------

PARALLEL C2	39 PF
PARALLEL L2	1000 NH
STRAY C2	10 PF
GATE OUTPUT RES	150 OHMS
PHASE SHIFT RES	50 OHMS
XC2	-102.0 OHMS, w/j
XL2	251.3 OHMS, w/j
XC-STRAY C2	-397.9 OHMS, w/j
NET X OF ALL C//L	-119 OHMS, w/j
Q	1.7
NET C-OUT	33 PF
RESONATE FREQ	22.7 MHZ
LOWER MODE	13.3 MHZ
% ABV LOW MODE	35.3%
FREQ OF NEXT O.T.	67 MHZ

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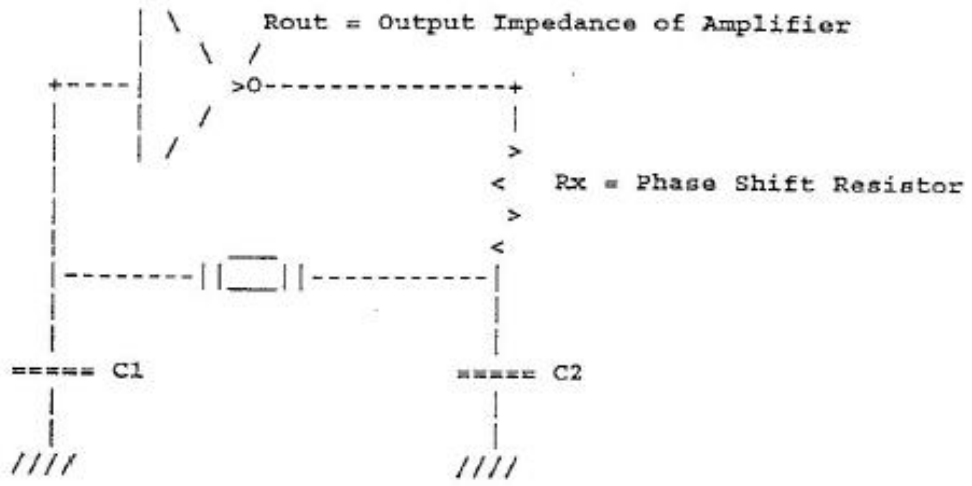
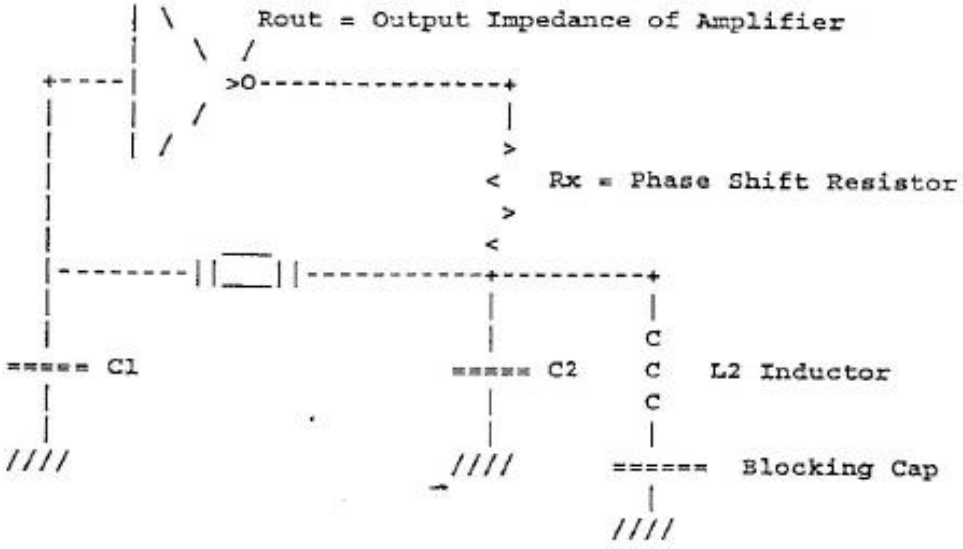
CIRCUIT FOR FUNDAMENTAL MODE OPERATION



CIRCUIT FOR PARALLEL TANK AT IC OUTPUT, CAPACITANCE ONLY AT INPUT.



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A1: [W17] "COPYWRITTEN by Raltron Elect. 2315 NW 107th Ave, Miami FL 33172
A2: U [W17] "Only Raltron has it all!  Crystals, Logic Clocks, VCXO, TCXO, OCXO Plus.
A3: [W17] "Call Marv Veeser at Raltron - (305) 593-6033.  Fax (305) 594-3973.
A5: [W17] 'This program is applicable for ASIC oscillator component selection.
A6: [W17] 'Program will calculate impedances for either parallel tank or series
A7: [W17] '    trap on either input or output of inverter.
A8: U [W17] "Use PageDown for applicable program, TAB for schematic, TAB TAB = Tables
A9: [W17] "Line 21:   Capacitance on ASIC output and input.  Fundamental only.
A10: [W17] "Line 41:   Cap on ASIC input.  Parallel tank on ASIC output.  Overtones.
A11: [W17] "Line 61:   Parallel tank on ASIC input.  Cap on ASIC output.  Overtones.
A12: [W17] "Line 81:   Cap on ASIC input.  Series trap on ASIC output.  3rd O.T.
A13: [W17] "Line 101:  Series trap on ASIC input.  Cap on ASIC output.  3 rd O.T.
A14: [W17] "Line 121:  Combinations of both parallel tank and series traps.  5+ O.T.
A15: [W17] "FOR BEST RESULTS:  Use reactances from 75 to 200 ohms.
A16: [W17] "   Estimate ASIC output impedance.  Set Q on output ckt = 1.5 minimum.
A17: [W17] "   For parallel tank, tune tank from 25% to 65% distance beetween lower
A18: [W17] "   mode and operating mode.  25%=max effective cap.  65% starts faster.
A19: [W17] "   Set voltage gain from ASIC output to ASIC input slightly above 1.
A20: [W17] '   WATCH THE NET CAPACITANCES ABOVE THE SOLID LINES ON INPUT & OUTPUT.
A21: U [W17] "CIRCUIT FOR FUNDAMENTAL MODE
A22: [W17] "  Enter Frequency, Stray CIN & Stray COUT, and GATE OUTPUT RESISTANCE.
A23: [W17] "  Itterate C1, C2 and Phase shift resistor (if available).
A24: [W17] "  VOLTAGE GAIN is NET C-OUT / NET C-IN.  Should be slightly above 1.
A25: [W17] "  PRACTICAL and CALCULATED LOAD are crystal load capacitance.
A27: [W17] "FREQ
B27: (F1) U [W8] 30
C27: [W11] 'MHZ
D28: [W18] '------- GATE OUTPUT CIRCUIT --------
D29: [W18] "C2
E29: U [W8] 27
F29: [W10] 'PF
D30: [W18] "STRAY C2
E30: (F0) U [W8] 10
F30: [W10] 'PF
A31: [W17] '------ GATE INPUT CIRCUIT --------
D31: [W18] "GATE OUTPUT RES
E31: U [W8] 150
F31: [W10] 'OHMS
A32: [W17] "C1
B32: (F0) U [W8] 22
C32: [W11] 'PF
D32: [W18] "PHASE SHIFT RES
E32: U [W8] 50
F32: [W10] 'OHMS
A33: [W17] "STRAY CIN
B33: (F0) U [W8] 8
C33: [W11] 'PF
D33: [W18] "XC2
E33: (F1) [W8] @IF(E29=0,"",-1/(2*@PI*B27*E29)*1000000)
F33: [W10] 'OHMS, w/j
A34: [W17] "XC1
B34: (F1) [W8] @IF(B32=0,"",-1/(2*@PI*B27*B32)*1000000)
C34: [W11] 'OHMS, w/j
D34: [W18] "XC-STRAY C2
E34: (F1) [W8] @IF(E30=0,"",-1/(2*@PI*B27*E30)*1000000)
F34: [W10] 'OHMS, w/j
A35: [W17] "XC-STRAY C1
B35: (F1) [W8] @IF(B33=0,"",-1/(2*@PI*B27*B33)*1000000)
C35: [W11] 'OHMS, w/j
D35: [W18] "NET X OF ALL C//L
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E35: (F0) [W8] -1/(2*@PI*B27*E37)*1000000
F35: [W10] 'OHMS, w/j
A36: [W17] "NET XC
B36: (F0) [W8] -1/(2*@PI*B27*B37)*1000000
C36: [W11] 'OHMS, w/j
D36: [W18] "Q
E36: (F1) [W8] (+E31+E32)/@ABS(E35)
F36: U [W10] @IF(E36<1,"NO GOOD","")
A37: [W17] "NET C-IN
B37: (F1) [W8] +B33+B32
C37: [W11] 'PF
D37: [W18] "NET C-OUT
E37: (F1) [W8] +E29+E30
F37: [W10] 'PF
A38: U [W17] '----------------------------------
D38: U [W18] '----------------------------------
A39: [W17] "VOLTAGE GAIN
B39: (F1) [W8] +E37/B37
C39: U [W11] @IF(B39<0.9,"TOO LOW",@IF(B39>1.8,"TOO HIGH",""))
D39: [W18] "XTAL LOAD, PRACT.
E39: (F0) [W8] (+E37-E30)*(B37-B33)/((E37-E30)+(B37-B33))+7
F39: [W10] 'PF
D40: [W18] "XTAL LOAD, CALC.
E40: (F0) [W8] +B37*E37/(B37+E37)
F40: [W10] 'PF
A41: U [W17] "CIRCUIT FOR PARALLEL TANK AT ASIC OUTPUT.
A43: [W17] "FREQ
B43: (F1) U [W8] 40
C43: [W11] 'MHZ
A44: [W17] "MODE
B44: U [W8] 3
C44: [W11] @IF(B44=3,"RD","TH")
D44: [W18] '-------- GATE OUTPUT CIRCUIT --------
D45: [W18] "PARALLEL C2
E45: U [W8] 39
F45: [W10] 'PF
D46: [W18] "PARALLEL L2
E46: (F0) U [W8] 1000
F46: [W10] 'NH
D47: [W18] "STRAY C2
E47: (F0) U [W8] 10
F47: [W10] 'PF
D48: [W18] "GATE OUTPUT RES
E48: U [W8] 150
F48: [W10] 'OHMS
A49: [W17] '------ GATE INPUT CIRCUIT --------
D49: [W18] "PHASE SHIFT RES
E49: U [W8] 50
F49: [W10] 'OHMS
A50: [W17] "C1
B50: (F0) U [W8] 22
C50: [W11] 'PF
D50: [W18] "XC2
E50: (F1) [W8] @IF(E45=0,"",-1/(2*@PI*B43*E45)*1000000)
F50: [W10] 'OHMS, w/j
A51: [W17] "STRAY CIN
B51: (F0) U [W8] 8
C51: [W11] 'PF
D51: [W18] "XL2
E51: (F1) [W8] @IF(E46=0,"",(2*@PI*B43*E46)*0.001)
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```
F51: [W10] 'OHMS, w/j
A52: [W17] "XC1
B52: (F1) [W8] @IF(B50=0,"",-1/(2*@PI*B43*B50)*1000000)
C52: [W11] 'OHMS, w/j
D52: [W18] "XC-STRAY C2
E52: (F1) [W8] @IF(E47=0,"",-1/(2*@PI*B43*E47)*1000000)
F52: [W10] 'OHMS, w/j
A53: [W17] "XC-STRAY C1
B53: (F1) [W8] @IF(B51=0,"",-1/(2*@PI*B43*B51)*1000000)
C53: [W11] 'OHMS, w/j
D53: [W18] "NET X OF ALL C//L
E53: (F0) [W8] @IF(E46=0,1/(1/(-1/(2*@PI*B43*(E45+0.1))*1000000)+1/(-1/(2*@PI*B43*(E47+0
F53: [W10] 'OHMS, w/j                                                    .1))*1000000)))
A54: [W17] "NET XC
B54: (F0) [W8] @IF(B50=0#AND#B51=0," C1 !!!",-1/(2*@PI*B43*B55)*1000000)
C54: [W11] 'OHMS, w/j
D54: [W18] "Q
E54: (F1) [W8] (+E48+E49)/@ABS(E53)
F54: U [W10] @IF(E54<1,"TOO LOW","")
A55: [W17] "NET C-IN
B55: (F0) [W8] +B51+B50
C55: [W11] 'PF
D55: [W18] "NET C-OUT
E55: (F0) [W8] -1/(2*@PI*B43*E53)*1000000
F55: [W10] 'PF
A56: U [W17] '----------------------------------
D56: U [W18] '----------------------------------
A57: [W17] "VOLTAGE GAIN
B57: (F1) [W8] @IF(B55=0,"C1 !!!",+E55/B55)
C57: U [W11] @IF(B57<0.9,"TOO LOW",@IF(B57>1.8,"TOO HIGH",""))
D57: [W18] "RESONATE FREQ
E57: (F1) [W8] @IF(E46=0,"",1/(2*@PI*@SQRT(E46*0.000000001*(E45*1.0000000E-12+E47*1.0000
F57: [W10] 'MHZ                                                  E-12))) +0,000001)
D58: [W18] "LOWER MODE
E58: (F1) [W8] @IF(B44<2.9,"",+B43*(B44-2)/B44)
F58: [W10] 'MHZ
A59: [W17] "XTAL LOAD, PRACT.
B59: (F0) [W8] (+E55-E47)*(B55-B51)/((E55-E47)+(B55-B51))+7
C59: [W11] 'PF
D59: [W18] "% ABV LOW MODE
E59: (P1) [W8] @IF(E46=0,"",(E57-E58)/(B43-E58))
F59: U [W10] @IF(E59>0.25#AND#E59<0.65,"," (NO GOOD)")
A60: [W17] "XTAL LOAD, CALC.
B60: (F0) [W8] +B55*E55/(B55+E55)
C60: [W11] 'PF
D60: [W18] "FREQ OF NEXT O.T.
E60: [W8] +B43*(B44+2)/B44
F60: [W10] 'MHZ
```