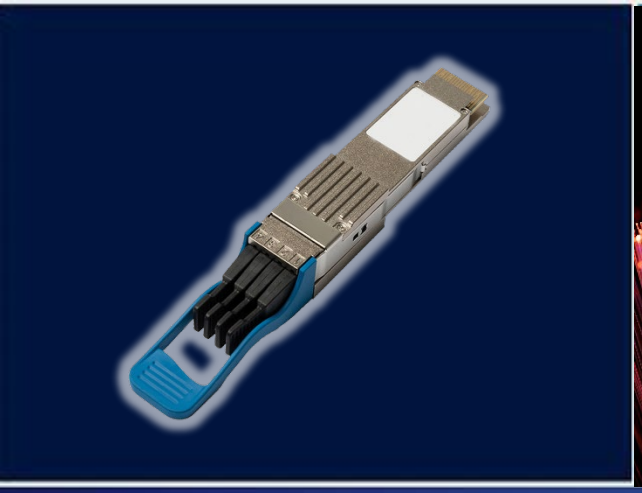
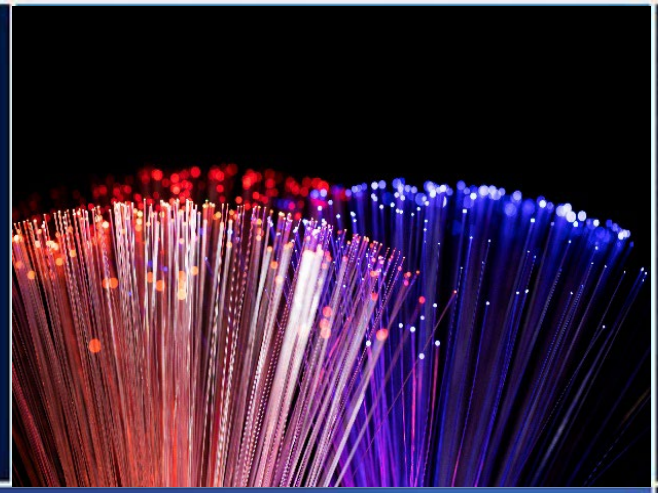




Frequency Components for Data Centers, Networking Equipment, and Optical Transceivers

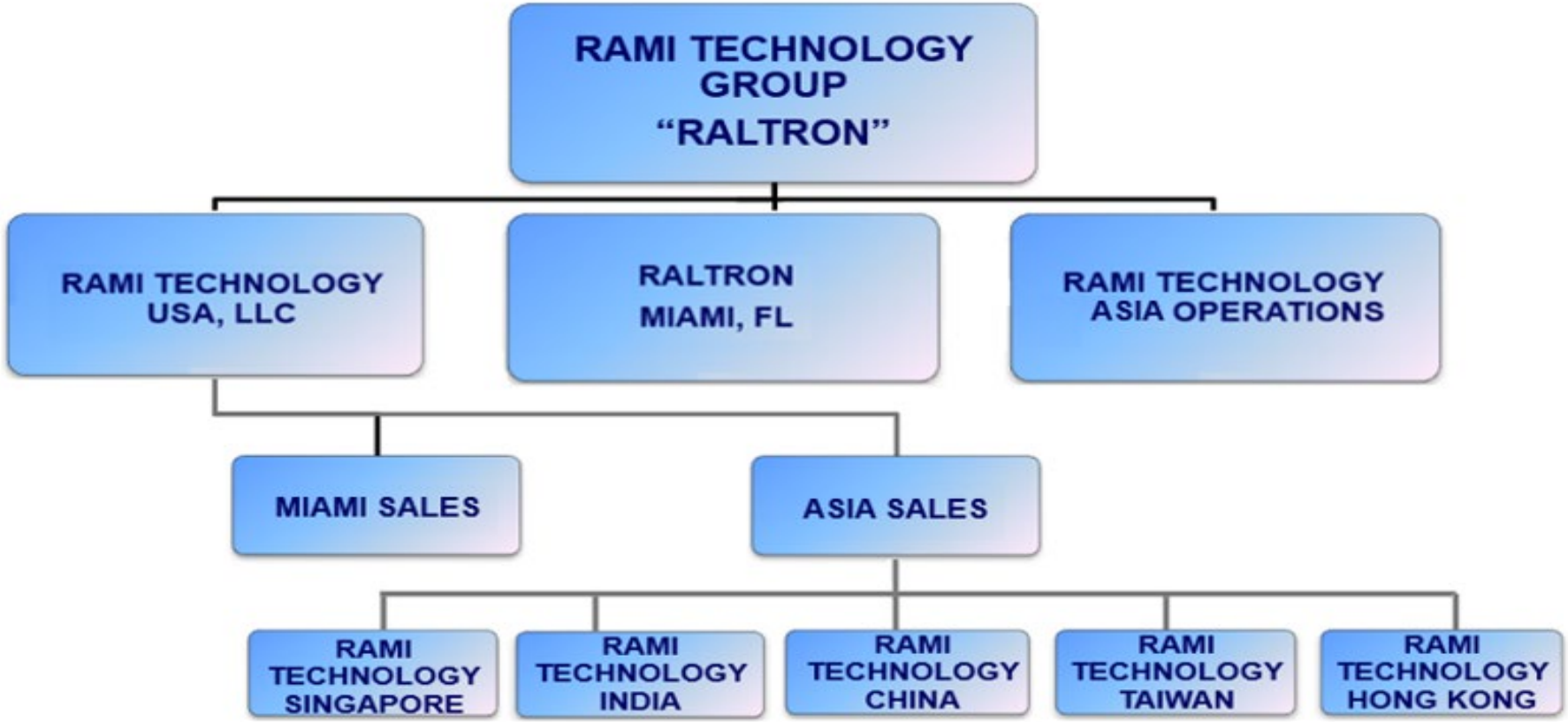
RALTRON

Raltron Electronics Introduction

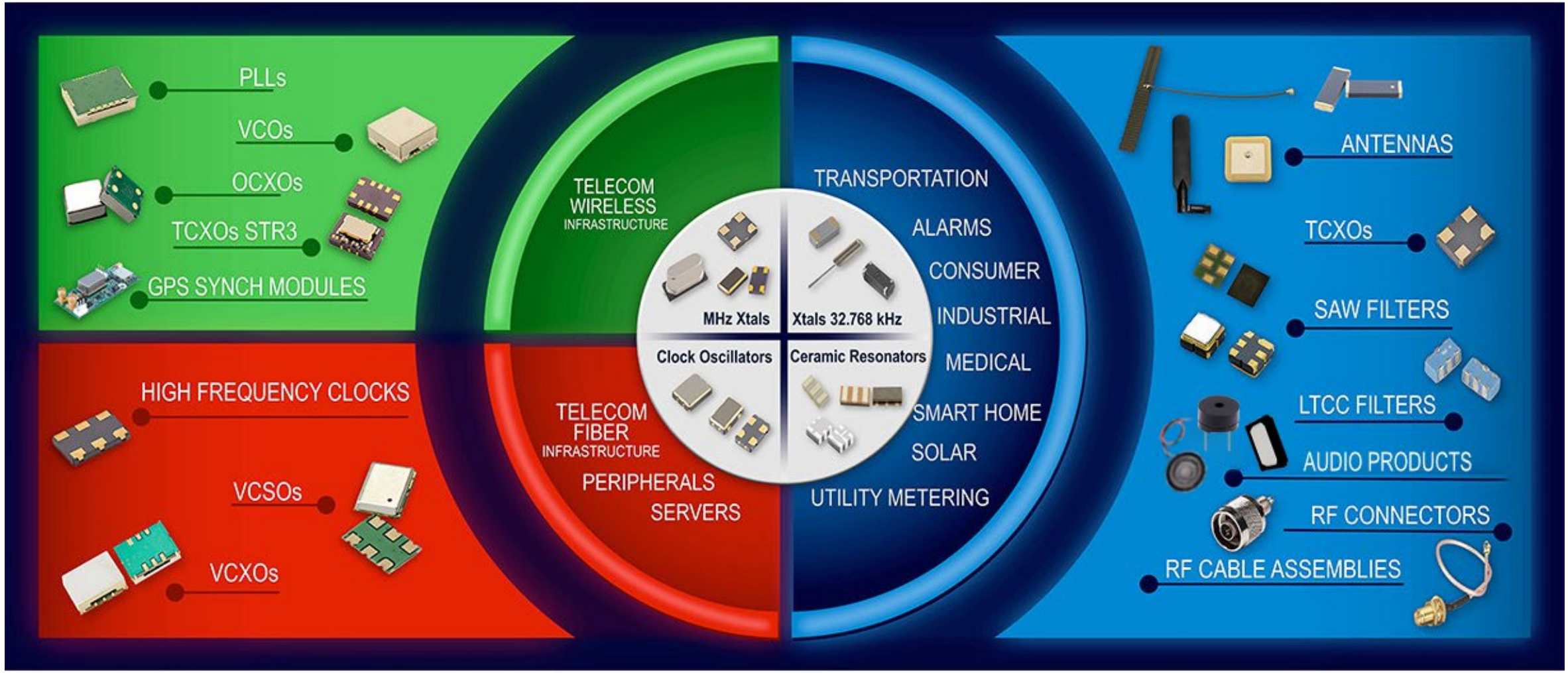
- Founded in 1983, headquartered in Miami ,Fl .
- Design, manufacturing and distribution of frequency management and IoT related products including:
  - Precision crystal oscillators (VCXO s, TCXOs, OCXO s), crystal and ceramic resonators.
  - Microwave components: VCO ' s , PLL 's, custom modules.
  - Filters(SAW, crystal).
  - LTCC products (filters, baluns, diplexers)
  - Antennas and RF Cable Assemblies
  - Audio Products
- Worldwide operations and distribution.
- Global presence through a network of sales offices, representatives and distributors.

Raltron Electronics Introduction

RALTRON / RAMI TECHNOLOGY GROUP

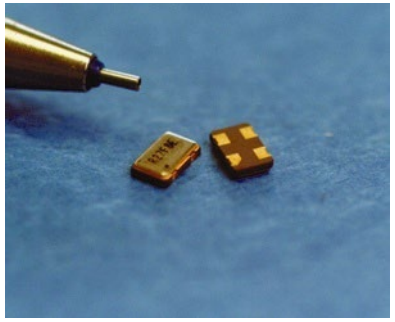


Product Portfolio



Technology Road Map – Clock Oscillators

SIZE (mm)	FREQUENCY
14 x 9.8 x 4.7	1 – 250 MHz
7.0 x 5.0 x 1.8	32.768 kHz, 1 – 1500 MHz
5.0 x 3.2 x 1.1	32.768 kHz, 1 – 1500 MHz
3.2 x 2.5 x 1.0	32.768 kHz, 1.8 – 300 MHz
2.5 x 2.0 x 0.8	32.768 kHz, 1 – 250 MHz
2.0 x 1.6 x 0.8	32.768 kHz, 1 – 250 MHz
1.6 x 1.2 x 0.3	2 - 80 MHz
1.2 x 1.0 x 0.3	2 – 80 MHz

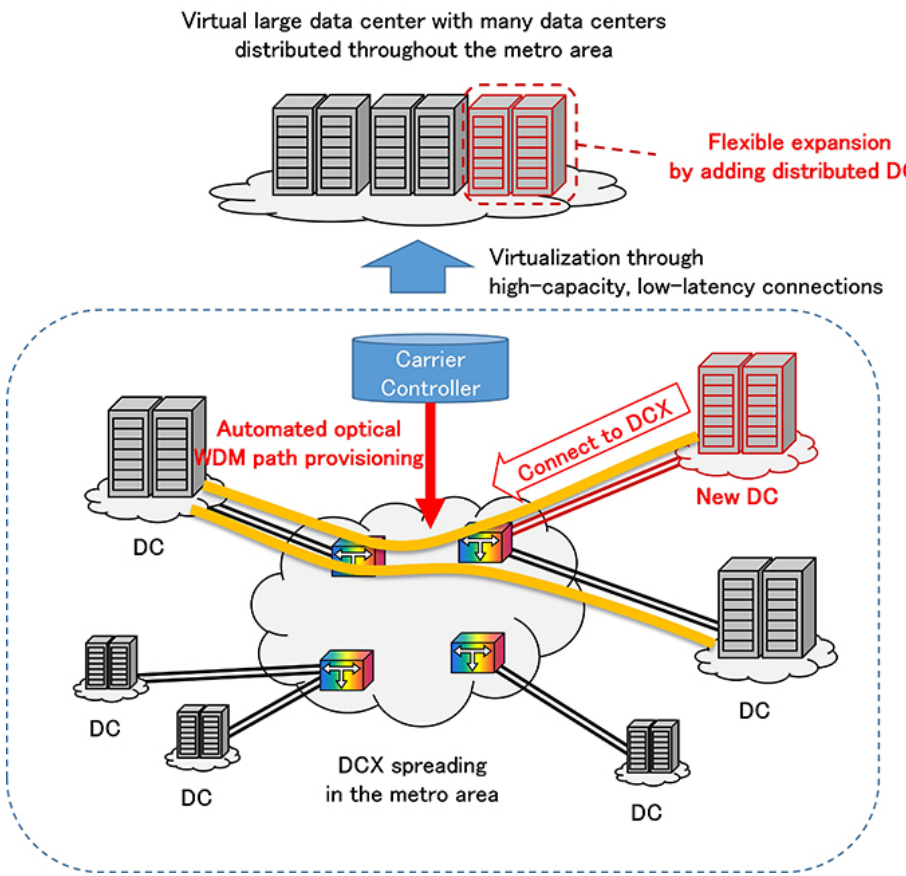


- Internal Construction: Fundamental Mode, PLL, 3rd OT, Analog Multiplication
- Stability: up to ±10ppm (all conditions) -40°C ~ +85°C
- Jitter: down to 50 fs (12kHz ~ 20MHz) RMS
- Low supply voltage: 1.8V, 2.5V, 3.3V
- Range supply voltage: 1.7V ~ 3.3V
- Output waveform: LVPECL, LVDS, HCMOS, HCSL
- Presence on references designs

APPLICATION

Industrial, Fiber Transmission, Wireless Transmission, Networking

Clock Oscillators Application: Data Centers - Servers

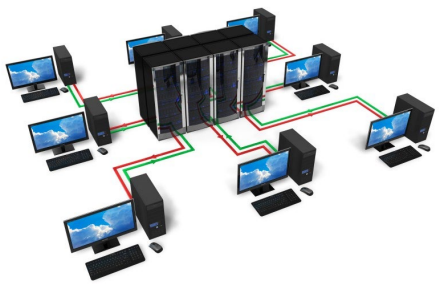


Performance needs

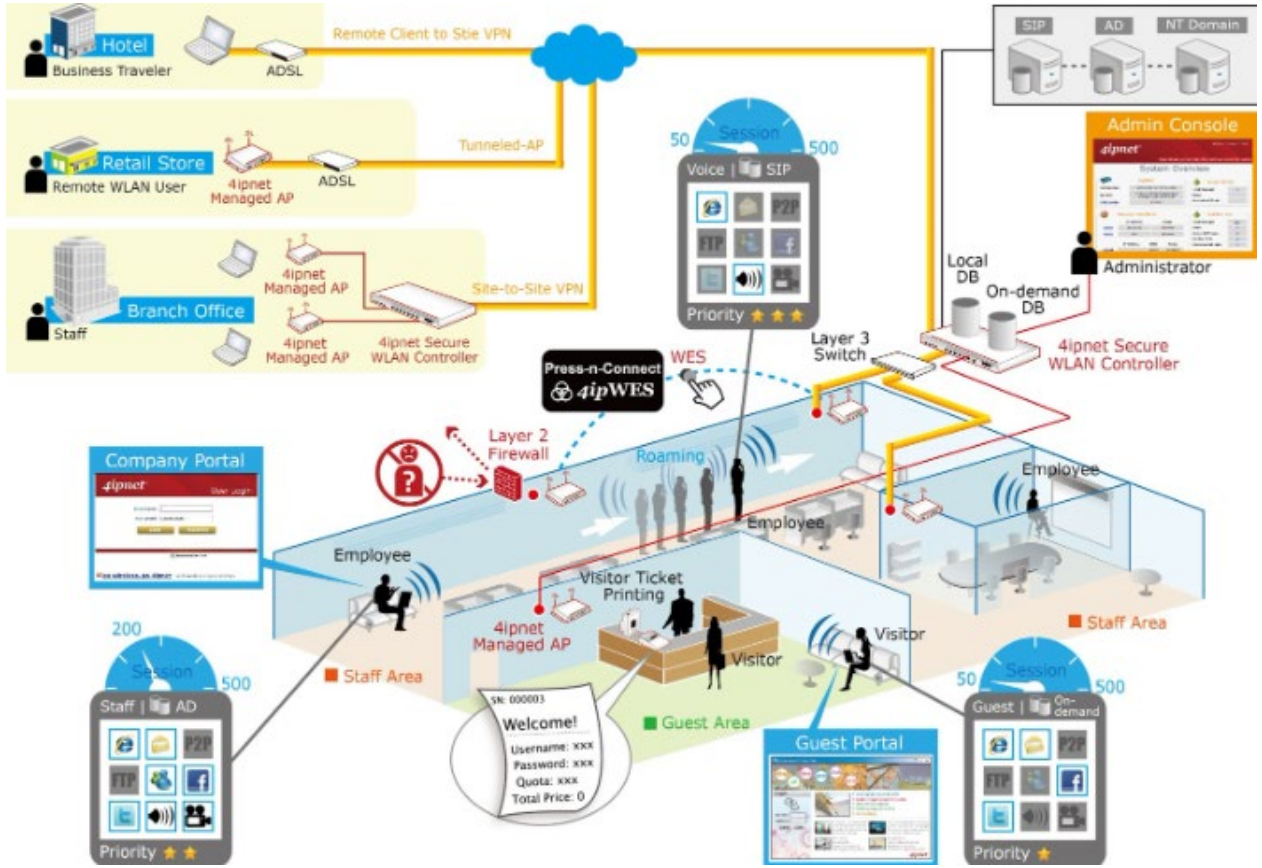
Low Phase Jitter – Down to 50fs (fundamental crystal)
Output Logic Options; HCMOS, LVPECL, LVDS and HCSL
Input Voltages; +1.8V, +2.5V, +3.3V
Frequency Stability ±25ppm
Operating Temperature, -40°C to +105°C
2.0x1.6mm, 2.5x2.0mm, 3.2x2.5mm packages

Cloud/Hybrid/On-premises servers

Web Server
FTP Server
File Server
Data Storage



Clock Oscillators Application: Network Solutions



Performance Needs

Low Phase Jitter – Down to 50fs (fundamental crystal)
Output Logic Options; HCMOS, LVPECL, LVDS and HCSL
Input Voltages; +1.8V, +2.5V, +3.3V
Frequency Stability ±25ppm
Operating Temperature, -40°C to +105°C
2.0x1.6mm, 2.5x2.0mm, 3.2x2.5mm packages

Applications

Wireless Infrastructure
Network Communications
Ethernet/Gbe/SyncE
SerDes
Fiber Channel - PON

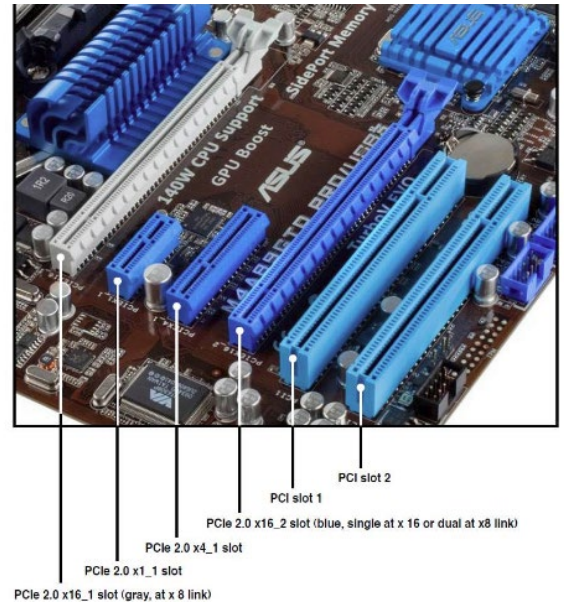
Clock Oscillators Applications: PCIe Express

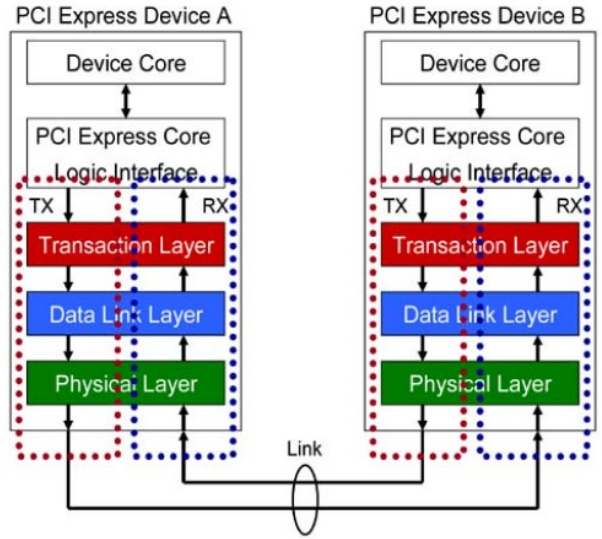
Performance Needs

HCSL Output Logic
Low Phase Jitter –Down to 50fs (fundamental crystal)
Input Voltages; +1.8V, +2.5V, +3.3V
Frequency Stability ±25ppm
Operating Temperature, -40°C to +105°C
2.0x1.6mm, 2.5x2.0mm, 3.2x2.5mm packages
Common Frequency - 100MHz

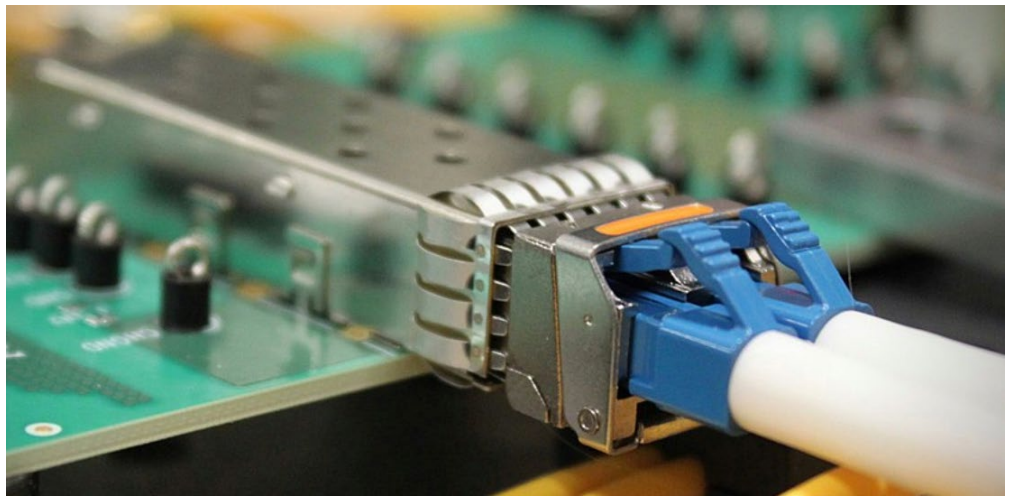
Applications

PCI Express [PCIe]
Data Storage Systems
Ethernet Line Cards
Serial ATA Express [SATAe]
AMD, TI, Intel, Mellanox, and Nvidia Chipsets





Clock Oscillator Applications: Fiber Optic Transceivers



Performance needs

Low Phase Jitter – Down to 50fs (fundamental crystal)
Output Logic Options; HCMOS, LVPECL, LVDS and HCSL
3 Voltage Options: +1.8V, +2.5V, +3.3V
Frequency Stability ±50ppm
Operating Temperature, -40°C to +105°C
2.0x1.6mm packages
Common Frequencies – 156.25MHz & 312.5MHz
PSRR – Better than 100 dB down at 1Mhz and higher
Differential Output Swing: 1.2V typ

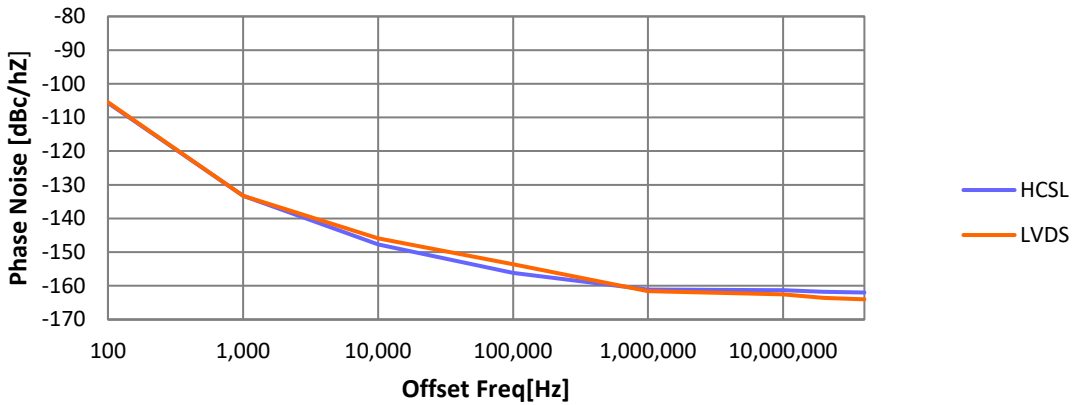
Output Characteristcs

Output	Symbol	Condition	min	typ	max	Unit
LVDS	Vo	Swing (Diff)	0.5	0.7	0.9	V
High Drive LVDS			0.8	1.2	1.6	
LVPECL			0.7	0.85	1	
HCSL			0.7	0.85	1	

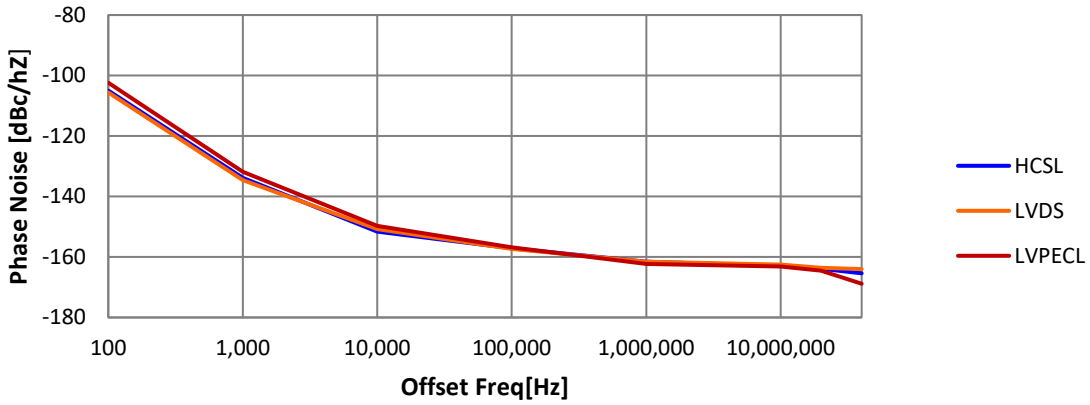
Chips Sets – Coherent (Finisar),Intel, Broadcom (Avago), Cisco (Acacia), InnoLight, Accelink, Eoptolink, Hisilicon, NeiPhotonics

Phase Noise Plots

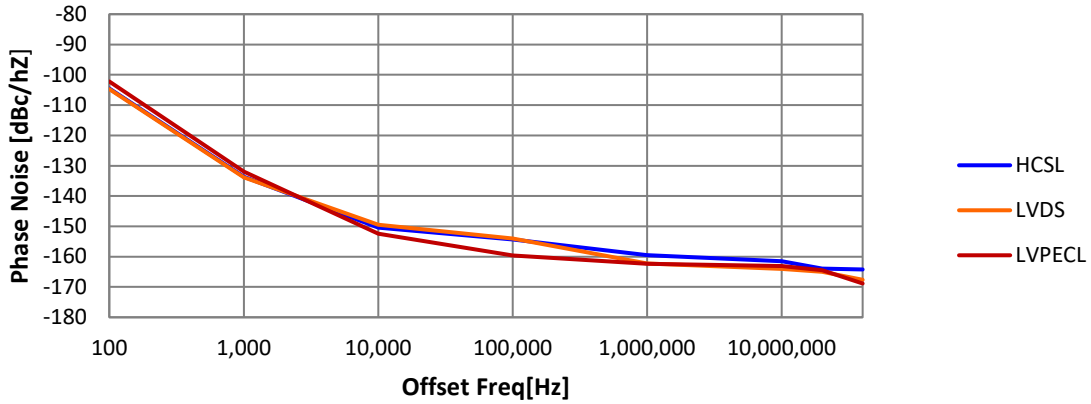
LVDS / HCSL at 1.8 VDC @ 156.25MHz
Fundamental Mode Crystal <50fs



LVDS / LVPECL / HCSL at 2.5 VDC @ 156.25MHz
Fundamental Mode Crystal <50fs

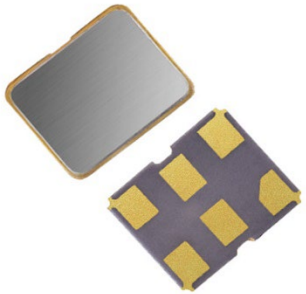


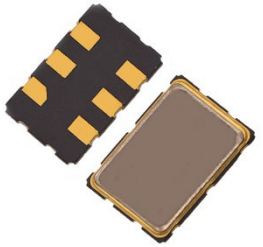
LVDS / LVPECL / HCSL at 3.3 VDC @ 156.25MHz
Fundamental Mode Crystal <50fs



Raltron Solutions – LVPECL/LVDS/HDLVDS/HCSL Clock Oscillators High Frequency Ultra Low Jitter

Specification	Specification Range	Features
Output Type	LVPECL – LVDS – HDLVDS-HCSL	Output type for Network and Server Bus
Package Sizes (mm)	3.2x2.5, 2.5x2.0, 2.0x1.6	Multiple footprint options
Voltage Options	1.8V (LVDS-HDLVDS) 2.5V, 3.3V	3 voltage options
Frequency Range	70MHz to 625MHz	
Temperature Stability	±20ppm -40 to +105°C	Excellent temperature stability and wide temperature range
Differential Output Swing	0.8V min / 1.2V typ / 1.6V max	Values only for High Drive LVDS
Common Frequencies	100MHz, 106.25MHz, 122.88MHz, 150MHz,153.6MHz, 156.250MHz, 159.375MHz, 161.1328125MHz, 187.5MHz, 200MHz, 212.5MHz, 312.5MHz, 625MHz	Common Server and Network Frequencies
Phase Jitter	Down to 30fs (fundamental crystal)	Excellent Jitter



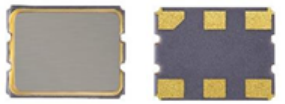


312.5 MHz Specification (LVPECL)

RALTRON
A RAMI TECHNOLOGY Company

LVPECL CLOCK OSCILLATOR

CP3225-312.500-3.3-50-X-T-TR



ELECTRICAL SPECIFICATION

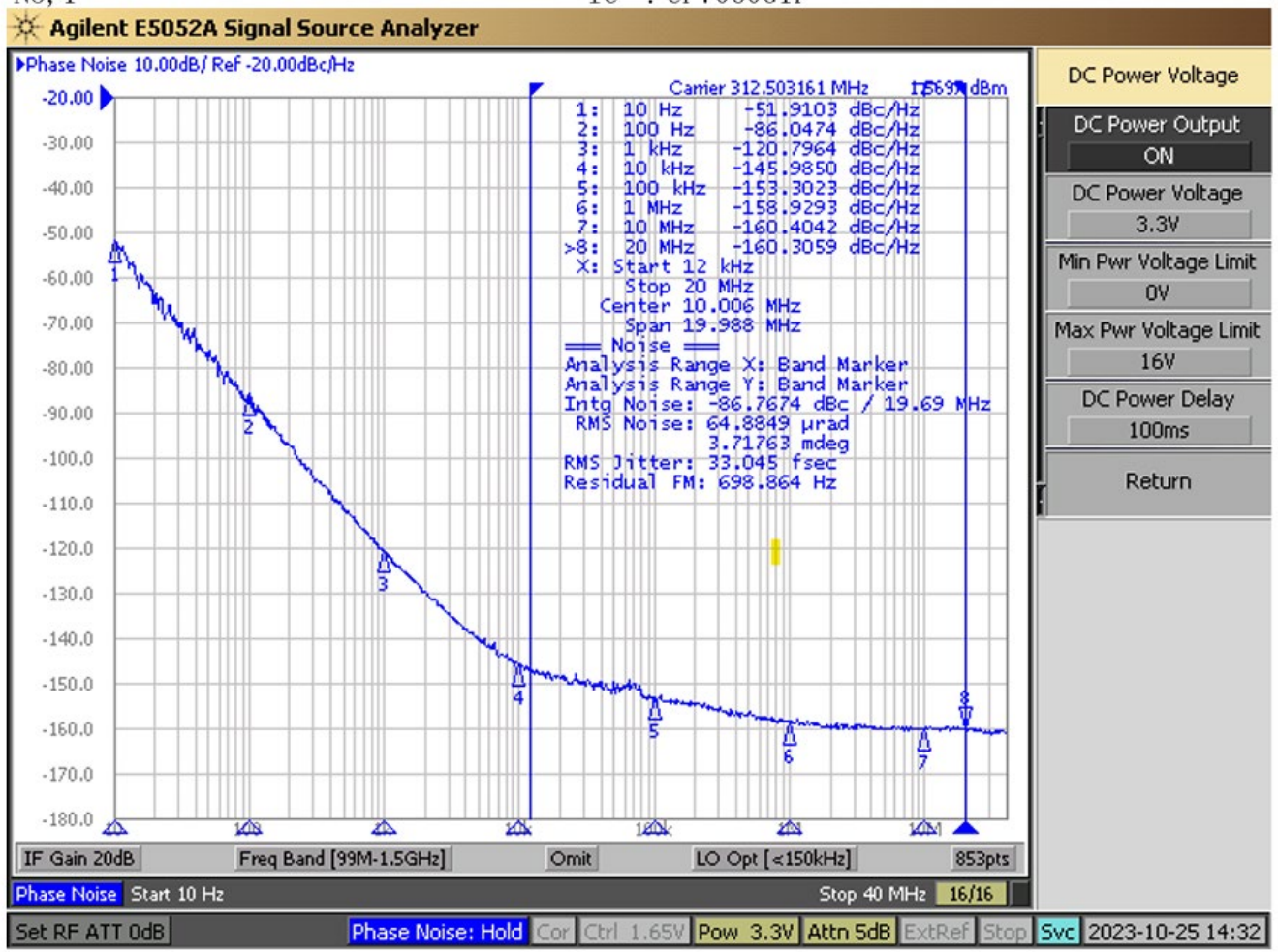
PARAMETER	SYMBOL	CONDITIONS	VALUE	UNIT
Nominal Frequency	fo	Ta=25°C	312.500	MHz
Supply Voltage	V_{CC}	Vcc ±10%	3.3	VDC
Supply Current, max	I_S	Vcc; Ta=+25°C;	70	mA
Operating Temperature Range	Ta	---	-40 ~ +85	°C
Storage Temperature Range	$T_{(stg)}$	Absolute max	-55 ~ +125	°C
Output Logic Type	---		LVPECL	-
Freq. Stability, max.	Δf/fo	Inclusive of 25°C Tolerance and Changes due to Operating Temperature, Supply Voltage, Load Variation and Aging	±50	ppm
Output Voltage	V_{OH}	Logic "1" Level	Vcc-1.085V min. to Vcc-0.880V max.	VDC
	V_{OL}	Logic "0" Level	Vcc-1.810V min. to Vcc-1.620V max.	VDC
Output Load	---	Connected between Out and Complementary Out	50	Ω
Enable / Disable Function	E/D	Pin 1: High, Pins 4 & 5 – Oscillation (Enabled), min	0.7 x Vcc	V
		Pin 1: Low, Pins 4 & 5 – High Impedance (Disabled), max	0.3 x Vcc	V
Symmetry (Duty Cycle)	DC	@50% Vdd	45 ~ 55	%
Rise and Fall Time, typ/max	tr / tf	@20% to 80% Vdd	400	ps
Standby Current, max	Ist		30	µA
Start up Time, max	T_{start}		10	ms
Differential Output Voltage, min			0.4	Vp-p
Jitter, RMS, typ	J	1σ, 12kHz < F_j < 20MHz	30	fs

312.5 MHz Phase Noise (LVPECL)

Frequency:312.500000MHz
Vdd: 3.3V
No, 1

Load:LVPECL
System:Agilent E5052A
IC : CF7060G1P

Size:3225



312.5 MHz Specification (HDLVDS)

RALTRON
A RAMI TECHNOLOGY Company

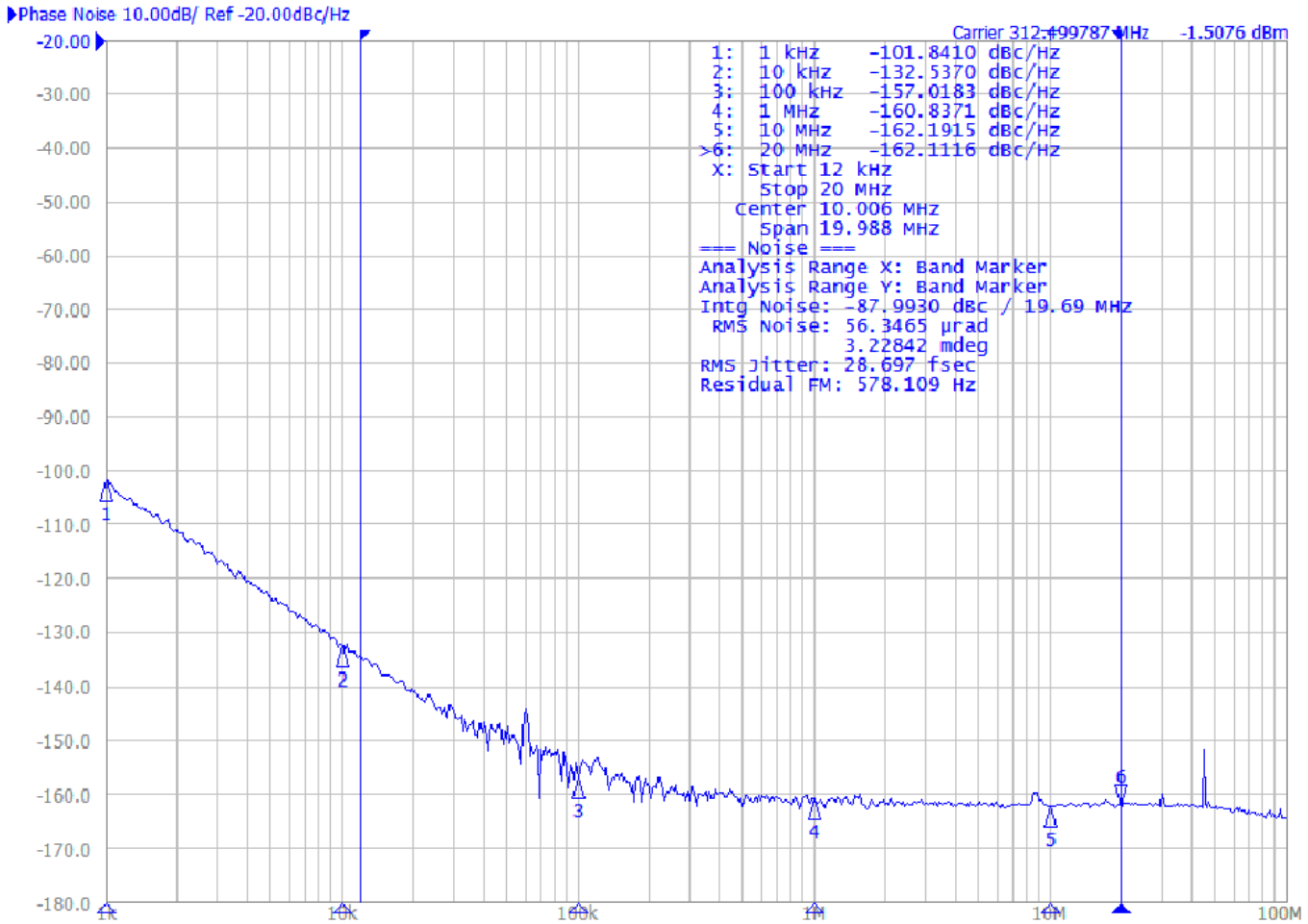
HIGH DRIVE
LVDS CLOCK OSCILLATOR

CLH2520-312.500-1.8-20-X6-T-TR-NS1

ELECTRICAL SPECIFICATION

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNIT
Nominal Frequency	fo	Ta=25°C	312.500	MHz
Supply Voltage	V_{CC}	Vcc ±5%	1.8	VDC
Supply Current, max	I_S	Vcc; Ta=+25°C;	135	mA
Freq. Stability, max	Δf/fo	Inclusive of 25°C Tolerance and Changes due to Operating Temperature, Supply Voltage, Load, First Year Aging	±20	ppm
Operating Temperature Range	Ta	---	-40 to +105	°C
Storage Temperature Range	$T_{(stg)}$	Absolute max	-55 to +125	°C
Output Logic Type	---		HDLVDS	
Differential Output Swing, min / typ			800 /1200	mV
Symmetry (Duty Cycle)	DC	@50% Vdd	45 to 55	%
Rise Time and Fall Time	tr / tf	@20% to 80% Vdd	175	ps
Output Load (*AC Coupled)	---	Connected between Out and Complementary Out	100	Ω
Enable / Disable Function	E/D	Pin 1: High, Pins 4 & 5 – Oscillation (Enabled), min	0.7 x Vcc	V
		Pin 1: Low, Pins 4 & 5 – High Impedance (Disabled), max	0.3 x Vcc	V
Standby Current	Ist		70	mA
Start Time			10	ms
Jitter, RMS, max	J	1σ, 12kHz < F_j < 20MHz	50	fs

312.5 MHz Phase Noise (HDLVDS)



625.0 MHz Specification (LVDS)

RALTRON
A RAMI TECHNOLOGY Company

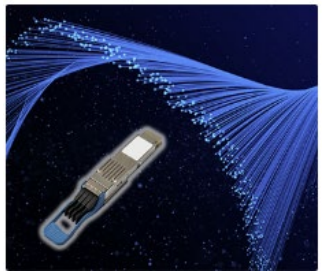
ULTRA LOW JITTER
LVDS CLOCK OSCILLATOR

CL3225-625.000-3.3-25-X-T-TR

ELECTRICAL SPECIFICATION

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNIT
Nominal Frequency	fo	Ta= +25°C	625.000	MHz
Supply Voltage	V_{CC}	Vcc ±5%	3.3	VDC
Supply Current, typ/max	I_S	Ta= +25°C	20, 40	mA
Operating Temperature Range	Ta		-40 ~ +85	°C
Storage Temperature Range	$T_{(stg)}$	Absolute max	-55 ~ +125	°C
Output Logic Type			LVDS	
Freq. Stability, max	Δf/fo	Inclusive of 25°C Tolerance and Changes due to Operating Temperature, Supply Voltage, Load, and First Year Aging	±25	ppm
Output Voltage, typ	V_{OH}		1.43	V
	V_{OL}		1.10	V
Output Offset Voltage, min/typ/max	V_{OS}		1.125/1.25/1.375	V
Output Offset Error, max			50	mV
Output Load	---	Connected between Out and Complementary Out	100	Ω
Enable / Disable Function	E/D	Pin 1: N.C. (Open) or High Pin 4 & 5 – Oscillation (Enabled), min	Vcc	V
		Pin 1: Low Pin 4 & 5 – High Impedance (Disabled), max	GND	V
Differential Output Voltage, min/typ			250/350	mV
Differential Output Error, max	ΔV_{OD}		50	mV
Symmetry (Duty Cycle)	DC	@50% Waveform	45 ~ 55	%
Rise Time / Fall Time, typ,max	tr / tf	@20% to 80% Waveform	300, 500	ps
Disable Delay Time, max			200	ns
Enable Delay Time, max			10	ms
Start-up Time, max	t_s		10	ms
Stand By Current, max			30	µA
RMS Phase Jitter, typ/max	J	1σ, 12kHz < F_j < 20MHz	20/30	fs

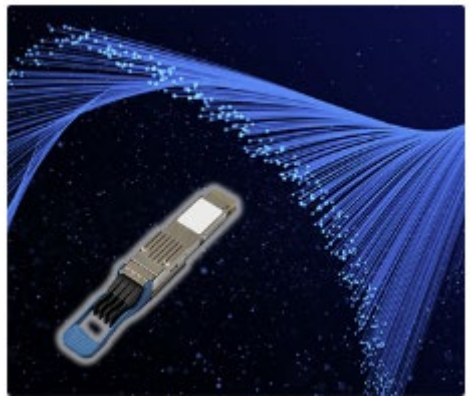
LVDS – MHz Clock Oscillators – Ultra Low Jitter Clock Oscillators - Optical Transceivers



Part Number	Size (mm)	Output	Oscillation Mode	Supply Voltage (V)	Frequency (MHz)	Stability (ppm)	Jitter (fs)
CLF2016-156.250-1.8-50-X-T-N1	2.0 x 1.6	LVDS	Fundamental	1.8	156.25	±50	47.8 typ
CLF2016-156.250-1.8-50-6-T-N1	2.0 x 1.6	LVDS	Fundamental	1.8	156.25	±50	47.8 typ
CLF2016-156.250-3.3-100-6-T-N11	2.0 x 1.6	LVDS	Fundamental	3.3	156.25	±100	50 max
CLF2016-156.250-J-50-X-T-N1	2.0 x 1.6	LVDS	Fundamental	2.5~3.3	156.25	±50	50 max
CLF2520-156.250-J-50-X-T-N1	2.5 x 2.0	LVDS	Fundamental	2.5~3.3	156.25	±50	50 max
CLF2520-156.250-1.8-50-X-T-N1	2.5 x 2.0	LVDS	Fundamental	1.8	156.25	±50	48.7 typ
CLF2520-156.250-1.8-50-6-T-N1	2.5 x 2.0	LVDS	Fundamental	1.8	156.25	±50	47.8 typ
CLF3225-156.250-1.8-50-X-T-N1	3.2 x 2.5	LVDS	Fundamental	1.8	156.25	±50	47.8 typ
CLF3225-156.250-J-50-X-T-N1	3.2 x 2.5	LVDS	Fundamental	2.5~3.3	156.25	±50	50 max
CLH2520-312.500-1.8-20-6-N31	2.5 x 2.0	LVDS	Fundamental	1.8	312.5	±20	50 max
CL2520-312.500-2.5-50-X-T-N2	2.5 x 2.0	LVDS	3rd Overtone	2.5	312.5	±50	50 max
CLF2520-312.500-3.3-50-X-T-N1	3.2 x 2.5	LVDS	Fundamental	3.3	312.5	±50	47.8 typ
CL3225-625.000-3.3-25-X-T-N2	3.2 x 2.5	LVDS	Fundamental	3.3	156.25	±25	30 max

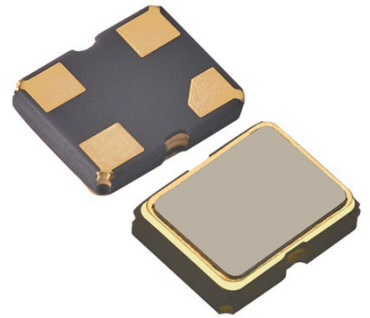
LVPECL – MHz Oscillators – Ultra Low Jitter Clock Oscillators – Optical Transceivers

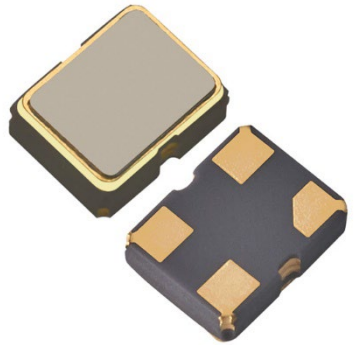
Part Number	Size (mm)	Output	Oscillation Mode	Supply Voltage (V)	Frequency (MHz)	Stability (ppm)	Jitter (fs)
CPF2016-156.250-3.3-50-6-T-N1	2.0 x 1.6	LVPECL	Fundamental	3.3	156.25	±50	50 max
CPF2016-156.250-J-50-X-T-N1	2.0 x 1.6	LVPECL	Fundamental	2.5~3.3	156.25	±50	50 max
CPF2520-156.250-3.3-50-X-T-N1	2.5 x 2.0	LVPECL	Fundamental	3.3	156.25	±50	70 max
CPF2520-156.250-3.3-50-6-T-N1	2.5 x 2.0	LVPECL	Fundamental	3.3	156.25	±50	50 max
CPF2520-156.250-J-50-X-T-N1	2.5 x 2.0	LVPECL	Fundamental	2.5~3.3	156.25	±50	50 max
CP3225-312.500-3.3-50-X-T-N2	3.2 x 2.5	LVPECL	3rd Overtone	3.3	312.5	±50	33 typ



Raltron Solutions – HCMOS Clock Oscillators

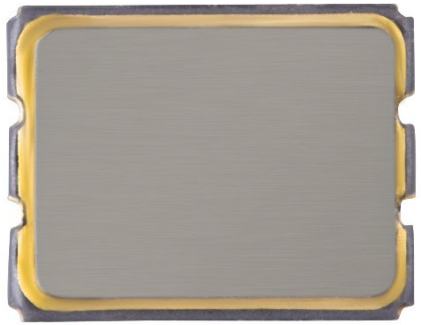
Specification	Specification Range	Features
Output Type	HCMOS	Output type for Network and Access Points
Package Sizes (mm)	2.5x2.0, 2.0x1.6,1.6x1.2	Multiple footprint options
Voltage Options	1.8V, 2.5V, 3.3V	3 voltage options
Frequency Range	70MHz to 220MHz	
Temperature Stabiltiy	±25ppm -40 to +105°C	Excellent temperature stability and wide temperature range
Common Frequencies	50MHz, 53.125MHz, 100MHz, 106.25, 122.88MHz, 150MHz 153.6MHz, 156.250MHz, 159.375MHz	Common Network Frequencies
Phase Jitter	Down to 150 fs	Excellent Jitter

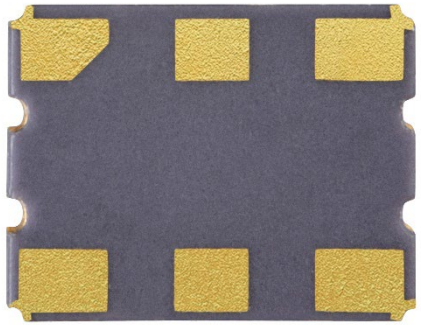




Raltron Solutions – HCSL Clock Oscillators

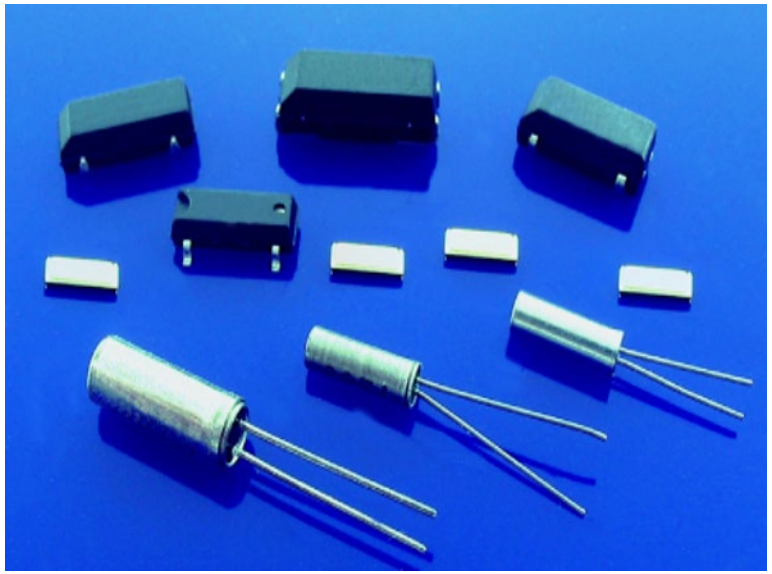
Specification	Specification Range	Features
Output Type	HCSL	Output type for PCIe Bus
Package Sizes (mm)	3.2x2.5, 2.5x2.0, 2.0x1.6	Multiple footprint options
Voltage Options	1.8V, 2.5V, 3.3V	3 voltage options
Frequency Range	27MHz to 220MHz	
Temperature Stabiltiy	±50ppm -40 to +105°C	Excellent temperature stability and wide temperature range
Common Frequencies	100MHz, 125MHz, 156.250MHz	Common PCIe frequencies
Phase Jitter	Down to 50fs (fundamental crystal)	Excellent Jitter





Technology Map – Tuning Fork

Package	Size (mm)	Freq (kHz)
Ceramic	4.1 x 1.5 x 0.9	32.768
	3.2 x 1.5 x 0.8	32.768
	2.0 x 1.2 x 0.6	32.768
	1.6 x 1.0 x 0.5	32.768
	1.2 x 1.0 x 0.4	32.768



Technology Map – Crystals SMD

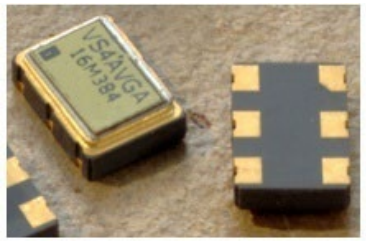
SIZE (mm)	FREQUENCY (MHz)
HC-49S-SMD	3 – 80
5.0 x 3.2 x 1.0	8 – 150
3.2 x 2.5 x 0.9	8 – 160
2.5 x 2.0 x 0.5	12 – 80
2.0 x 1.6 x 0.5	16 – 80
1.6 x 1.2 x 0.3	24 – 80
1.2 x 1.0 x 0.3	30 – 80

- **Smaller Packages**
  - Down to 1.2 x 1.0 x 0.3 mm
- **Improved Stability**
  - Down to ±10 ppm -40°C ~ +**105**°C
- **Higher Frequencies**
  - ~ 300 MHz Fundamental

Technology Road Map – VCXO-VCSO

VCXO

SIZE (mm)	FREQUENCY (MHz)
9.0 x 14 x 5 (SAW)	125 – 800
9.0 x 14 x 5 (Crystal)	1 – 1500
5.0 x 7.0 x 1.5 (Crystal)	1 – 1500
5.0 x 3.2 x 1.0 (Crystal)	1 – 1500

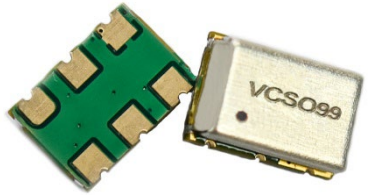


- Internal Construction: Fundamental Mode, PLL, 3rd OT, Analog Multiplication, SAW
- Temperature Stability: to ±20ppm (all conditions)
- APR (absolute pull range): to ±150ppm
- Low Jitter: down to 50fs (12kHz ~ 20MHz) RMS
- Low Phase Noise: down to -175dBc /Hz Noise Floor
- Output Waveform: LVPECL, LVDS, LVCMOS, HCSL

APPLICATION

SONET/SDH, Networking, SD/HD video, Test Instrument, Clock and Data recovery, Clock Generation

VCSO



SIZE (mm)	FREQUENCY (MHz)
7.0 x 5.0	400 – 1000

- Internal Construction: Fundamental Mode
- Supply Voltage: 3.3V
- APR (absolute pull range): ±50ppm max
- Low Jitter: down to 0.03ps (12kHz ~ 20MHz) RMS
- Phase Noise: -156dBc /Hz Noise Floor
- Output Waveform: LVPECL

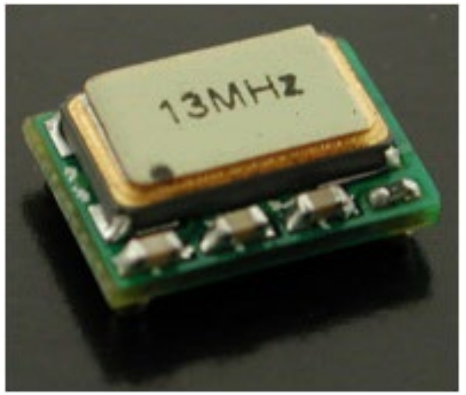
APPLICATION

400 GHz Ethernet,, SD/HD video, Test Instrument, Clock and Data recovery, Clock Generation,Metro

Technology Map – Stratum III SMD VCTCXO/TCXO

•STRATUM III

SIZE (mm)	FREQUENCY (MHz)	VOLTAGE (VDC)	Frequency Stability -40 to +85°C	OUTPUT WAVEFORM
5.0 x 7.0 x 1.5	10 - 52	2.5 to 5.0	0.20 ppm	Clipped Sine Wave & CMOS
5.0 x 3.2 x 1.5	10 - 52	2.7 to 5.5	0.20 ppm	Clipped Sine Wave & CMOS



- Tighter Stability: to ± 0.1 ppm, -10° C ~ + 60° C
- Stratum 3 Compliant: ± 0.28 ppm over - 40° C ~ + 85° C
  ± 4.6 ppm overall including 20 years Aging
- Low Phase Noise Performance: -135 dBc /Hz at 1 kHz and -150 dBc/Hz on the floor

- Low Power Substitute for OCXO for short haul applications
- 5G Open RAN and Backhaul applications

Quick Summary – Raltron OCXO's

SIZE (package)	FREQUENCY (MHz)
TH DIP 14	1 – 100
SMD DIP 14 style	1 - 100
TH 2x2x1	10 – 300
TH Euro	1 – 160
SMD 1.0x0.9x0.5	1 – 160
SMD 9 x 14	10 – 50
SMD 9 x 7	5 – 40

- Smallest Packages: 9 x 7 mm OCXO
- Frequency Range: 1 to 300.000 MHz
- Best Temperature Stability: ± .1 ppb (-40°C to +85°C)
- Aging: 0.5ppb/day / 50ppb/1st year
- Thru Hole and Surface Mount

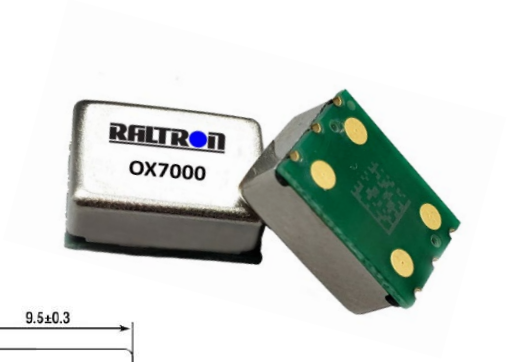
Phase Noise, typ	**-130dBc/Hz**	**10 Hz**
	-150dBc/Hz	**100 Hz**
	-160dBc/Hz	**1kHz**
	-170dBc/Hz	**10kHz**

Typical Values for 10MHz OCXO

APPLICATION

Telecommunication, Base Stations, Test and Measurement Equipment, IEEE 1588

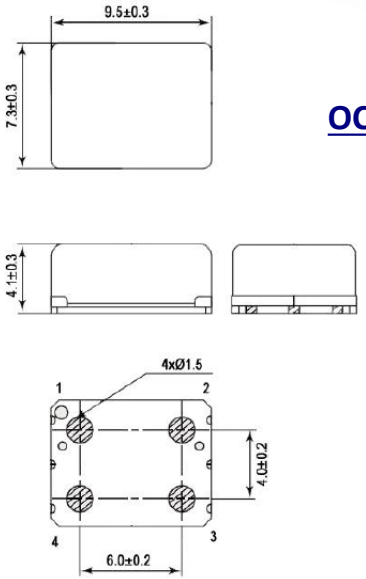
OCXO 9x7 mm



Electrical Specifications

PARAMETER	SYMBOL	CONDITION	VALUE			UNIT
			Min.	Typ.	Max.	
Frequency Range*	f_o		5.000		40.000	MHz
Nominal Frequencies		10, 12.8, 13, 19.2, 20, 25, 25.6, 30.72, 38.88, 40				MHz
Supply Voltage	V_s	Vs ±5%	3.135	3.3	3.465	V
Power Consumption	P_S	Steady state, @ 25°C		0.35	0.5	W
	$P_{S,w}$	During warm-up ,@ 25°C		0.8	0.9	
Warm-up Time	t_W	Vs, Ta=+25°C, within ±100ppb of final frequency with reference after 1 hour on			3	min
Frequency Calibration	$\Delta f/f_0$	Ta=+25°C, Vc at center, before shipment	-500		+500	ppb
Frequency Stability vs. Temperature*	$\Delta f/f_0$ (T_a)	Over Operating temperature range	-10		+10	ppb
Frequency Stability vs. Supply Voltage	$\Delta f/f_0$ (ΔVcc)	Ta=25°C, Vs±5%	-10	±5	+10	ppb
Aging, after 30 days of operation	$\Delta f/\Delta t_d$	Per day	-5		+5	ppb
	$\Delta f/\Delta t_y$	First year	-300		+300	ppb
Operating Temperature Range*			-40		+85	°C
Storage Temperature Range	$T_{(stg)}$		-40		+85	°C
Control Voltage Range	V_C		0.2	1.5	2.8	V
Frequency Tuning Range	$\Delta f/f$		±5			ppm
Slope		Positive	-	-	-	-

*Not any Combination Frequency-Operating Temperature Range- Stability is available. Please consult factory



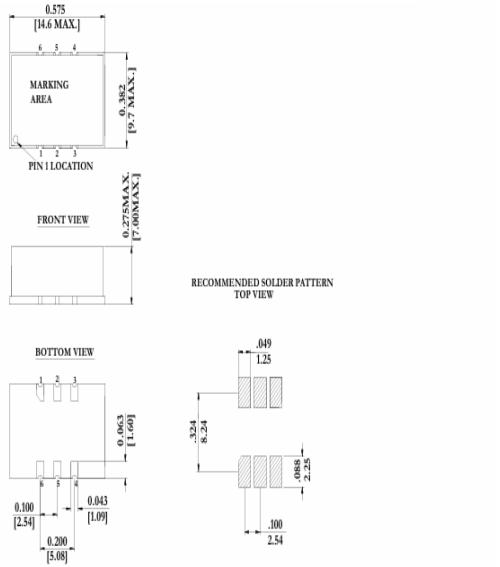
OCXO SERIES 7000

PIN	SYMBOL	FUNCTION
1	N/C or V_c	No connect or Voltage Control
2	GND	Ground
3	OUTPUT	Output
4	Vcc	Supply Voltage

OCXO 9 X 14 mm

Electrical Specifications

PARAMETER	SYMBOL	CONDITION	VALUE			UNIT
			Min.	Typ.	Max.	
Frequency Range*	f_o		10.000		50.000	MHz
Supply Voltage	V_s	Vs ±5%	3.135	3.3	3.465	V
			4.75	5.0	5.25	
Power Consumption	P_S	Steady state, @ 25°C			1.5	W
	$P_{S,w}$	During warm-up ,@ 25°C			2.5	W
Warm-up Time	t_W	Vs, Ta=+25°C, within ±100ppb of final frequency with reference after 1 hour on			5	min
Frequency Calibration	$\Delta f/f_0$	Ta=+25°C, after 15mins power on ref. to nominal frequency	-200		+200	ppb
Frequency Stability vs. Temperature*	$\Delta f/f_0$ (T_a)	Measurement referenced to (fmax+fmin)/2. See Table	-5		+5	ppb
Frequency Stability vs. Supply Voltage	$\Delta f/f_0$ (ΔV_{CC})	Ta=25°C, Vs±5%, load=15pF	-5		+5	ppb
Frequency Stability vs. Load Variation	$\Delta f/f_0$ (Δl)	Ta=25°C, Vs, load=15pF±5%	-5		+5	ppb
Aging, after 30 days of operation	$\Delta f/\Delta t_d$	Per day	-3.0		+3.0	ppb
	$\Delta f/\Delta t_y$	First year	-500		+500	ppb
	$\Delta f/\Delta t_y$	10 years	-3		+3	ppm
Operating Temperature Range*		See Table 1	-40		+85	°C
Storage Temperature Range	$T_{(stg)}$		-40		+105	°C
Short Term Stability		τ=1s			0.05	ppb
Control Voltage Range	V_C		0	1.65	3.0	V
Frequency Tuning Range		V_C = 0V	-4		-2	ppm
		V_C = 1.65V	-200		+200	ppb
		V_C= 3.3V	+2		+4	ppm
Linearity			-10		+10	%



PIN	SYMBOL	FUNCTION
1	N/C or V_C	No connector or Control Voltage
2	N/C	No connect
3	GND	Case/Ground
4	OUTPUT	RF Output
5	N/C	No connect
6	Vs	Supply Voltage

Contact

http://www.raltron.com
Raltron Electronics
10400 N.W. 33rd Street
Miami, FL 33172, U.S.A.
Phone: 305 593 6033
Fax: 305 594 3973