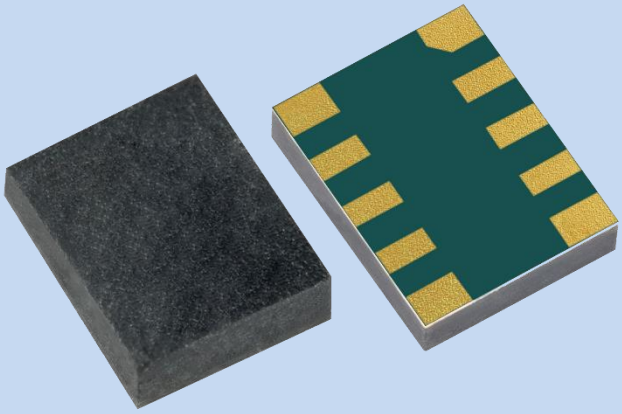
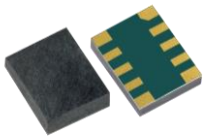


REAL TIME CLOCK MODULE

RTT24134

RTT24134

Real Time Clock Module

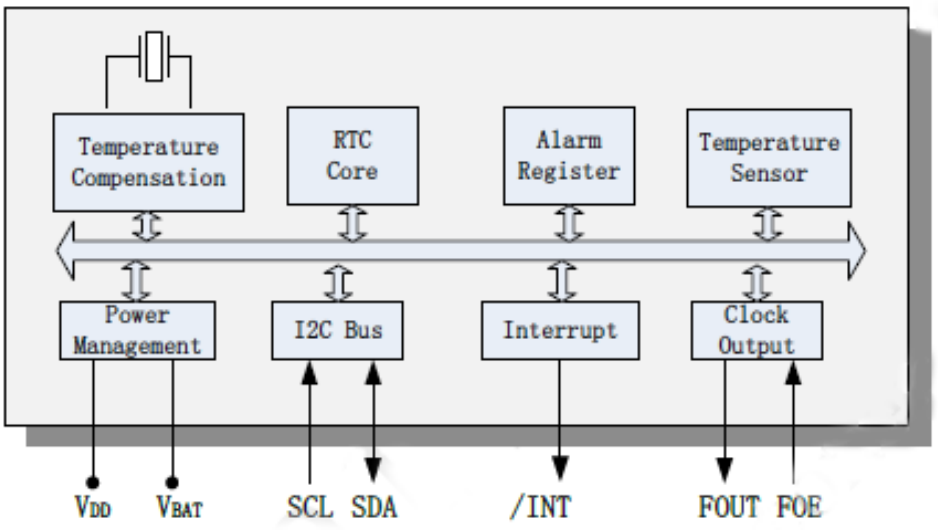


RTT24134 is a high-accuracy I2C bus interface real-time clock with low power consumption. It embeds a 32.768kHz TCXO. The high precise temperature sensor and temperature compensated circuit ensure the high clock accuracy. It supports calendar (year, month, day, hour, minute, second), clock and timer functions etc. The SMD3225 package with only 1.0mm thickness makes it very suitable to be used in portable and small size electronic devices .

KEY FEATURES

- Low current consumption: 1.0uA (Typ.)
- High stability:
  ±3.4ppm @-40~+85℃
- Build-in TCXO: 32.768kHz
- Communication interface: I²C bus
- Power supply voltage: 1.6V~5.5V
- Build-in temperature sensor
- Operation Temperature Range: -40℃ ~ +85℃
- Leap years autocorrection
- Timer output function with adjustable period
- Package: 3.2mm × 2.5mm × 0.9mm
- Backup battery switchover function

BLOCK DIAGRAM



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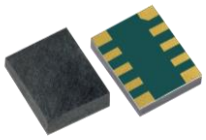


ELECTRICAL SPECIFICATIONS

1.1 Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{DD}		-0.3		6.5	V
Backup Battery Voltage	V_{BAT}		-0.3		6.5	V
Input Voltage	V_{IN}	FOE, SCL, SDA Input	GND-0.3		6.5	V
Clock Output Voltage	V_{OUT1}	FOUT	GND-0.3		V_{DD}+0.3	V
Output Voltage	V_{OUT2}	SDA, /INT	GND-0.3		6.5	V
Storage Temperature	T_{STG}		-55		+125	℃

1.2 Recommended Operating Conditions

Table 2. Recommended Operating Conditions

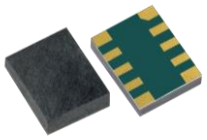
Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Power Supply Voltage (normal mode)	V_{DD}		2.5	3.0	5.5	V
Power Supply Voltage In case of single supply (VDD = VBAT)	V_{DD}		1.6	3.0	5.5	V
Backup Battery	V_{BAT}		1.6	3.0	5.5	V
Current Consumption	I_{DD}	Using Battery supply only		1.0		uA
Operation Temperature	T_{OPR}		-40	25	+85	℃

Note:

1 : To apply Min. value of VDD and VBAT, VCORE need to be supplied with more than 2.5V at least for the oscillation to stabilize (oscillation start time tSTA).

2 : After powered off, ensure that VDD = VBAT = GND for more than 10 seconds before next power on

3 : If there is no special indication, the test conditions are GND = 0V, VDD = Vbat = 2.5V ~ 5.5V, Ta = - 40 ℃ ~ + 85 ℃.



1.3 Frequency Characteristics

Table 3. Frequency Characteristics

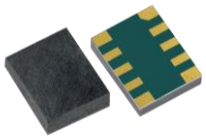
Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Frequency Stability	Δf/f	-40℃ ~ +85℃	-3.4		+3.4	ppm
Oscillation Start Time	tSTA	@25℃			1	s
Year Aging	fa	@25℃, First year	-3		+3	ppm
Temperature Sensor Accuracy	Temp	V_{DD}=3.0V	-5		+5	℃
FOUT duty cycle	$t_{w/t}$		40	50	60	%

Note: If there is no special indication, the test conditions are GND= 0V, $V_{DD=}$ Vbat=2.5V ~ 5.5V, Ta=-40~+85℃

1.4 DC Characteristics

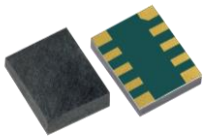
Table 4. DC Characteristics

Parameter	Symbol	Condition		Value			Unit
				Min.	Typ.	Max.	
Average Current consumption1	IDD1	V_{DD}=5.0V	fSCL=0Hz, FOE=GND, /INT = VDD; VDD=VBAT; FOUT off (High-Z); Compensation interval 2s; VDD voltage detection time 2ms		1.25	5.1	uA
Average Current consumption 2	IDD2	V_{DD}=3.0V			1.0	4.9	uA
Average Current consumption 3	IDD3	V_{DD}=5.0V	fSCL=0Hz, FOE=VDD, /INT = VDD; VDD=VBAT; FOUT:32.768kHz, CL=0pF; Compensation interval 2s; VDD voltage detection time 2ms		5.8	20	uA
Average Current Consumption 4	IDD4	V_{DD}=3.0V			3.8	19	uA
High-level input voltage	V_{IH}	SCL, SDA, FOE pin		0.8 x V_{DD}		5.5	V
Low-level input voltage	V_{IL}			GND-0.3		0.2 x V_{DD}	V
High-level output voltage	V_{OH1}	V_{DD}=5.0V, I_{OH} = -1mA		4.0		5.0	FOUT pin
	V_{OH2}	V_{DD}=3.0V, I_{OH} = -1mA		2.2		3.0	
	V_{OH3}	V_{DD}=3.0V, I_{OH} = -100μA		2.9		3.0	
Low-level output voltage	V_{OL1}	V_{DD}=5.0V, I_{OL} = 1mA		GND		GND+0.5	FOUT pin



Note: If there is no special indication, the test conditions are GND=0V, VDD=1.6V~5.5V, Ta=-40°C~+85°C.

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Low-level output Voltage	V_{OL2}	V_{DD}=3.0V, I_{OL} = 1mA	GND		GND+0.8	FOUT pin
	V_{OL3}	V_{DD}=3.0V, I_{OL} = 100uA	GND		GND+0.1	FOUT pin
	V_{OL4}	V_{DD}=5.0V, I_{OL} = 1mA	GND		GND+0.25	/INT pin
	V_{OL5}	V_{DD}=3.0V, I_{OL} = 1mA	GND		GND+0.4	/INT pin
	V_{OL6}	V_{DD}≥3.0V, I_{OL} = 3mA	GND		GND+0.4	SDA pin
Input leakage current	I_{LK}	FOE, SDA, SCL pin, V_{IN} = V_{DD} or GND	-0.5		0.5	uA
Output leakage current	I_{OZ}	FOUT, SDA, /INT pin, V_{IN} = V_{DD} or GND	-0.5		0.5	uA



1.5 AC Characteristics

Table 5. AC Characteristics

VDD =2.5V ~ 4.5V; Ta=-40℃ ~ +105℃

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
SCL clock frequency	fSCL				400	kHz
SCL low level time	tLOW		1.3			us
SCL high level time	tHIGH		0.6			us
Start condition setup time	tHD;STA		0.6			us
Start condition hold time	tSU;STA		0.6			us
Stop condition setup time	tSU;STO		0.6			us
Bus idle time between start condition and stop condition	tRCV		1.3			us
Data setup time	tSU;DAT		100			ns
Data hold time	tHD;DAT		0			ns
SCL, SDA rising time	tr				0.3	us
SCL, SDA falling time	tf				0.3	us

Note: Note: when the master accesses the equipment through I²C bus, all communication from sending start condition to sending stop shall be completed within 1 second. If it exceeds 1 second, the I²C bus interface will be reset through the internal bus timeout function.

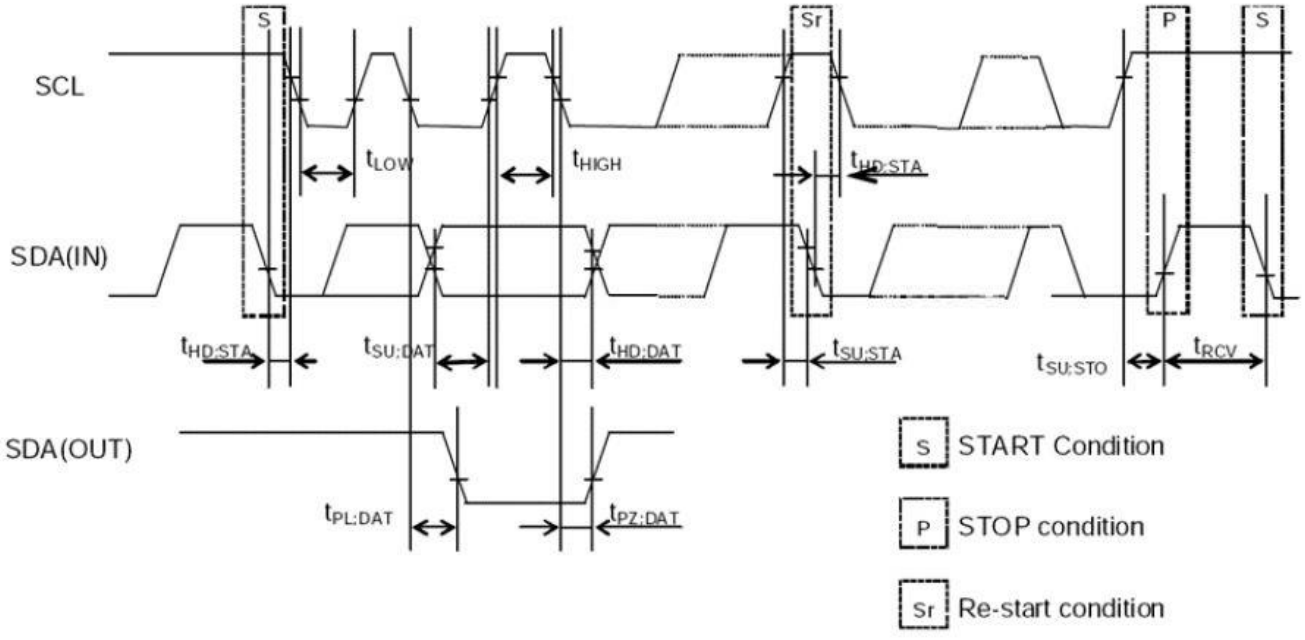
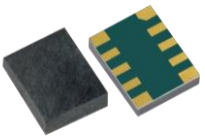


Figure 1. I²C bus Timing Chart



2.1 Register Lists

Address 0x00~0x0F: Basic Time and Calendar Registers
Address 0x10~0x1F: Extended Register Group 1
Address 0x20~30: Extended Register Group 2
Note: 0x10~16 and 0x00~06 with the same function, 0x1B~1F and 0x0B~0F with the same function

Table 6. Basic Time and Calendar Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x00	SEC	o	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				R/W
0x01	MIN	o	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				R/W
0x02	HOUR	o	o	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				R/W
0x03	WEEK	o	6	5	4	3	2	1	0	R/W
0x04	DAY	o	o	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				R/W
0x05	MONTH	o	o	o	BCD code, Month tens place, 0-1	BCD code, month ones place, 0-9				R/W
0x06	YEAR	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9				R/W
0x07	RAM	●	●	●	●	●	●	●	●	R/W
0x08	MIN Alarm	AE	BCD code, Minute tens place, 0-5			BCD code, Minutes ones place, 0-9				R/W
0x09	Hour Alarm	AE	●	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				R/W
0x0A	WEEK Alarm	AE	6	5	4	3	2	1	0	R/W
	DAY Alarm		●	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				R/W
0x0B	Timer Counter 0	128	64	32	16	8	4	2	1	R/W
0x0C	Timer Counter 1	●	●	●	●	2048	1024	512	256	R/W
0x0D	Extension Register	TEST	WADA	USEL	TE	FSEL[1]	FSEL[0]	TSEL[1]	TSEL[0]	R/W
0x0E	Flag Register	o	o	UF	TF	AF	o	VLF	VDET	R/W
0x0F	Control Register	CSEL[1]	CSEL[0]	UIE	TIE	AIE	o	o	RESET	R/W

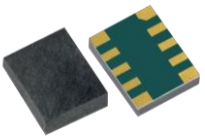
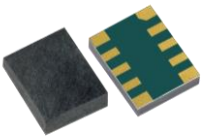


Table 7. Extended Register Group 1

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x10	SEC	o	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				R/W
0x11	MIN	o	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				R/W
0x12	HOUR	o	o	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				R/W
0x13	WEEK	o	6	5	4	3	2	1	0	R/W
0x14	DAY	o	o	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				R/W
0x15	MONTH	o	o	o	BCD code, Month tens place, 0-1	BCD code, Month ones place, 0-9				R/W
0x16	YEAR	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9				R/W
0x17	TEMP	128	64	32	16	8	4	2	1	R
0x18	Backup Function	o	o	o	o	VDET OFF	SWOFF	BKSMP [1]	BKSMP [0]	R/W
0x19	Not use	o	o	o	o	o	o	o	o	R
0x1A	Not use	o	o	o	o	o	o	o	o	R
0x1B	Timer Counter 0	128	64	32	16	8	4	2	1	R/W
0x1C	Timer Counter 1	●	●	●	●	2048	1024	512	256	R/W
0x1D	Extension Register	TEST	WADA	USEL	TE	FSEL [1]	FSEL [1]	TSEL [1]	TSEL [0]	R/W
0x1E	Flag Register	o	o	UF	TF	AF	o	VLF	VDET	R/W
0x1F	Control Register	CSEL [1]	CSEL [0]	UIE	TIE	AIE	o	o	RESET	R/W

Table 8. Extended Register Group 2

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x20	Device	Vendor ID [3:0]				VER[3:0]				R
0x21	Control Register 1	Reserved: Ensure to be 0x8				○	○	○	VBATSW	R/W
0x22-26	RSV	Reserved: Ensure to be 0x00								R
0x27	SubSEC	Reserved				SubSEC[3:0]				R
0x28-30	RSV	Reserved: Ensure to be 0x00								R/W



Note:

1. After power-up reset or in case VLF bit returns "1", make sure to initialize all registers to default state before using the RTC. Ensure all inputs are in the required range and the defined values are set for the reserved bits in case the clock cannot work normally.

- During the initial power-up, below bits will be in the state as below:
  Initial 0:TEST, WADA, USEL, TE, FSEL[1:0], TSEL[0], UF, TF, AF, CSEL[1], UIE, TIE, RESET, VDETOFF, SWOFF, BKSMP[1:0], VBATSW.
  Initial 1: VLF, VDET, CSEL[0].

- All other register values are undefined, so make sure to reset the module before using it.
- The bits marked with "○" can be read out "0" only after initializing.
- The bits marked with "●" are RAM bits which can be used to write or read any data.

- Only 0 can be written to UF, TF, AF, VLF, VDET bits.

- Make sure "0" to be written for TEST bits which are used for testing only.

- Reserved bits must be set to the defined values accordingly.

2.2 Details of Registers

2.2.1 Clock Counter Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x00/10	SEC	○	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				0x00
0x01/11	MIN	○	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				0x00
0x02/12	HOUR	○	○	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				0x00

SEC: BCD format, Value: 0~59

MIN: BCD format, Value: 0~59

HOUR: BCD format, Value: 0~23

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x13	WEEK	○	6	5	4	3	2	1	0	0x40

WEEK: Value 01h, 02h, 04h, 08h, 10h, 20h, 40h. Only one bit can be set to 1 each time, all others must be set to 0.

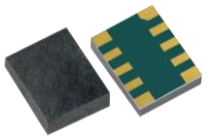


Table 9. WEEK Register

WEEK	Data	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sunday	01h	0	0	0	0	0	0	0	1
Monday	02h	0	0	0	0	0	0	1	0
Tuesday	04h	0	0	0	0	0	1	0	0
Wednesday	08h	0	0	0	0	1	0	0	0
Thursday	10h	0	0	0	1	0	0	0	0
Friday	20h	0	0	1	0	0	0	0	0
Saturday	40h	0	1	0	0	0	0	0	0

.

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x14	DAY	O	O	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				0x01

DAY: BCD format, the value range will be adjusted automatically according to the month setting and if a leap year or not .

Table 10. DAY Register Value

Month	Day Value Range
1, 3, 5, 7, 8, 10, 12	1~31
4, 6, 9, 11	1~30
February in normal year	1~28
February in leap year	1~29

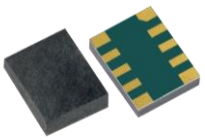
Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x05	MONTH	O	O	O	BCD code, Month tens place, 0-1	BCD code, Month ones place, 0-9				0x01
0x06	YEAR	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9				0x00

MONTH: BCD format, Value 1~12

YEAR: BCD format, Value 0~99(2000~2099)

Example: 2020/01/01 Wednesday 21:18:36

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x00/10	SEC	O	0	1	1	0	1	1	0
0x01/11	MIN	O	0	0	1	1	0	0	0
0x02/12	HOUR	O	O	1	0	0	0	0	1
0x03/13	WEEK	O	0	0	0	1	0	0	0
0x04/14	DAY	O	O	0	0	0	0	0	1
0x05/15	MONTH	O	O	O	0	0	0	0	1
0x06/16	YEAR	0	0	1	0	0	0	0	0



2.2.2 Alarm Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x08	MIN Alarm	**AE**	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				0x00
0x09	HOUR Alarm	**AE**	●	BCD code, Hour tens place, 0-2		BCD code, Minute ones place, 0-9				0x00
0x0A	WEEK Alarm	**AE**	6	5	4	3	2	1	0	0x00
	DAY Alarm		●	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				

According to AIE, AF, WADA bits setting, the alarm interrupt will be generated once the current time match the settings in the above registers, the /INT pin goes to low level and AF bit is set to '1' to record an alarm interrupt event has occurred.

WEEK Alarm/DAY Alarm: Controlled by WADA bit in 0x0D register.

AE: Alarm Enable bit, 0-enable; 1-disenable.

AF: Defined in 0x0E register bit3.

AIE: Defined in 0x0F register bit3.

2.2.3 Timer Control Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x0B/1B	Timer Counter 0	128	64	32	16	8	4	2	1	0x00
0x0C/1C	Timer Counter 1	●	●	●	●	2048	1024	512	256	0x00

According to TE, TF, TIE, TSEL[1:0] bits setting, a timer interrupt will be generated once the value counts down to 0 from the one set in the above registers.

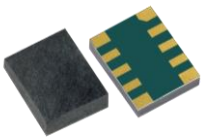
TE: Defined in 0x0D register bit4

TF: Defined in 0x0E register bit4.

TIE: Defined in 0x0F register bit4.

TSEL[1:0]: Defined in 0x0D register bit1 and bit0

2.2.4 Extension Registers



Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x0D/1D	Extension Register	TEST	WADA	USEL	TE	FSEL[1]	FSEL[0]	TSEL [1]	TSEL [0]	0x02

TEST: Test bit, must be set to "0"
WADA: WeekAlarm/DayAlarm control bit, decide 0x0A register as DAY Alarm or WEEK Alarm. 0-WEEK alarm, 1-DAY alarm
USEL: Update Interrupt Select bit, 0-output interrupt once a second, 1-output interrupt once a minute
TE: Timer Enable bit, 0-disenable, 1-enable; Timer counter can update new config when TE from "0" to "1"

FSEL[1], FSEL[0]: FOUT frequency setting:

FSEL[1]	FSEL[0]	FOUT Frequency
0	0	32.768kHz (Default)
0	1	1024Hz
1	0	1Hz
1	1	off

TSEL[1], TSEL[0]: Timer countdown period(source clock) setting:

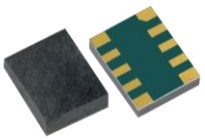
TSEL[1]	TSEL[0]	Source clock
0	0	4096Hz
0	1	64Hz
1	0	1Hz
1	1	1/60Hz

2.2.5 Flag Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x0E/1E	Flag Register	○	○	UF	TF	AF	○	VLF	VBFF	0x03

UF: Update flag bit. When time update interrupt event occurs, it will be set to "1" and keeps "1" until a "0" is written to it.
TF: Timer Flag bit. When a fixed-cycle timer interrupt event occurs, it will be set to "1" and keeps "1" until a "0" is written to it.
AF: Alarm Flag bit. When an alarm interrupt event occurs, it will be set to "1" and keeps "1" until a "0" is written to it.
VLF: Voltage Low Flag bit. When supply voltage is lower than 1.4V, it will be set to "1" and keeps "1" until a "0" is written to it.
VDET: Voltage Detection Flag bit. When supply voltage is lower than 2.1V, it will be set to "1" and keeps "1" until a "0" is written to it.

2.2.6 Control Registers



Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x0F	Control Register	CSEL[1]	CSEL[0]	UIE	TIE	AIE	o	o	RESET	0x40

CSEL[1], CSEL[0]: Compensation interval Select 1, 0 bits, used to set temperature compensation interval.

CSEL[1]	CSEL[0]	Compensation Interval
0	0	0.5s
0	1	2s(default)
1	0	10s
1	1	30s

UIE: Update Interrupt Enable bit. When UF changes from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disenable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).
TIE: Timer Interrupt Enable bit: When TF changes from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disenable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).
AIE: Alarm Interrupt Enable bit: When AF changes from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disenable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).
RESET: Reset IC, prepared for the synchronized starting of time or timer.

2.2.7 Temperature Register

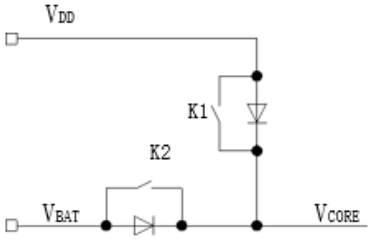
Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x17	TEMP	128	64	32	16	8	4	2	1	0x0

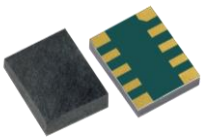
Read digital temperature data, Temp [℃] = TEMP *4 *0.1839-55.155.

2.2.8 Battery Backup Switchover Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x18	Backup Function	o	o	o	o	VDET OFF	SWOFF	BKSMP [1]	BKSMP[0]	0x00

This register controls the power switchover function. Once abnormal VDD is detected, it will be switched to use battery as the power supply.
The power circuit diagram is shown below:





VDETOFF (Voltage Detector OFF): Main power supply VDD voltage detection control bit. 0-enable detection function (Default), VDD voltage will be detected once a second; 1-disenable detection function.
SWOFF (Switch OFF): Switch K1 control bit. 0- close (Default); 1- open
BKSMP[1], BKSMP[0](Backup mode Sampling time): Control the voltage detection sampling time. Default: 00.

Table10 V_{DD} Voltage Sampling Time

VDD Detect Function	VDETOFF	SWOFF	BKSMP [1]	BKSMP [0]	V_{DD} Voltage Sampling Time	Switch K1 ON/OFF	Notes
ON	0	X	0	0	2ms	2ms OFF	Default
			0	1	16ms	16ms OFF	
			1	0	128ms	128ms OFF	
			1	1	256ms	256ms OFF	
OFF	1	0	x	x	OFF	ON	K1 Close
		1	x	x	OFF	OFF	K1 Open

2.2.9 Device ID Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x20	Device ID	Vendor ID[3:0]				Ver[3:0]				0XD2

VendorID[3:0]: The fixed value is defined as VendorID[3:0]=1101b=Dh to represent RALTRON. Ver[3:0]: version of the IC

2.2.10 Control Register 1

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x21	Control Register 1	Reserved: must be 0x8				Ver[3:0]			VBATSW	0x80

VBATSW: Battery supply switch K2 control bit. Default 0, 0- Open, 1-Close.

2.2.11 Sub-second Timer Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x27	SubSEC	Reserved				SubSEC[3:0]				0x00

SubSEC[3:0]: sub second bit, and unit is 1/16s.

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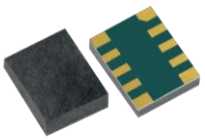
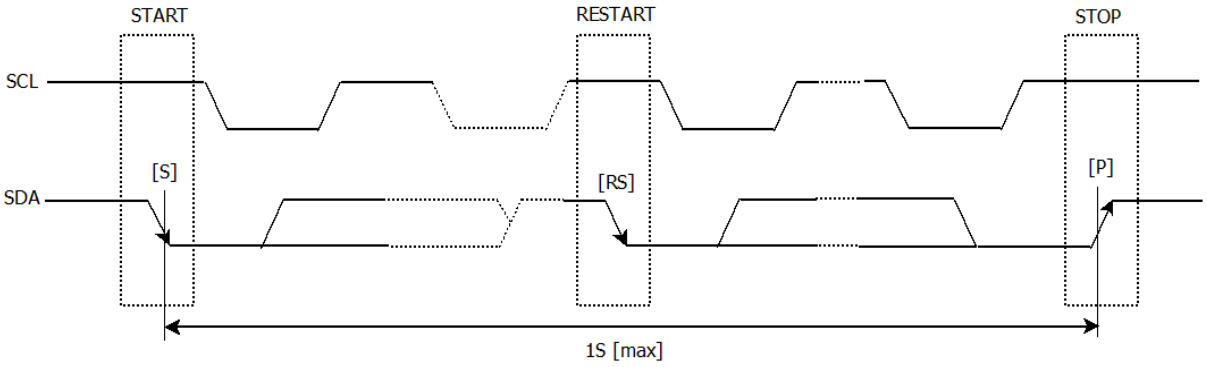




I²C bus supports bi-directional communications through a serial clock line SCL and a serial data line SDA. I²C bus device can be defined as "Master" and "Slave". **RTT24134** can only be used as Slave.

3.1 Cautions

I²C bus includes START, RESTART, STOP conditions, the duration between START and STOP must be less than 1 second just in case the bus to be set to standby mode automatically. A new START condition must be transferred before restarting of any communications.

RTT24134 I²C bus interface supports single byte read/write operations as well as multiple bytes incremental access. After 0xFF address, the next one will be 0x00.

3.2 Slave Address

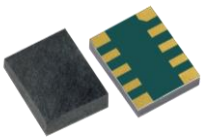
Table 11. I²C Bus Slave Address

Transfer data	Slave address							R/W
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
65h (Read)	0	1	1	0	0	1	0	1 (Read)
64h (Write)								0 (Write)

RTT24134 I²C bus Slave Address is [0110 010*].

3.3 I²C bus Protocol

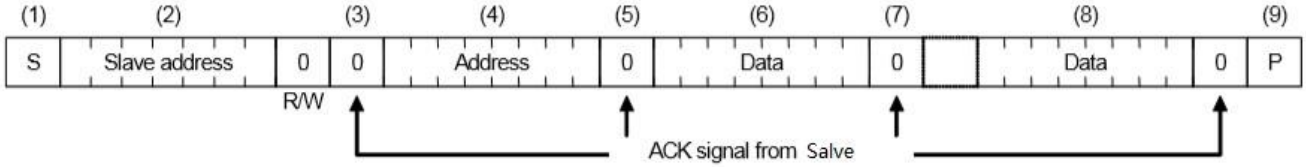
It is assumed CPU is master and **RTT24134** is slave in this section.



3.3.1 Write Process

I²C bus includes an address auto-increment function, once the initial address has been specified, the **RTT24134** increments (+1) the address automatically after each data is sent, then to write next data.

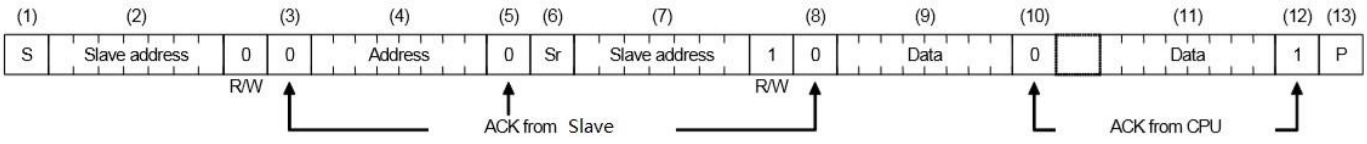
(1) CPU sends start condition[S]
(2) CPU sends **RTT24134**'s slave address with R/W bit to set to write mode
(3) CPU verifies ACK signal from **RTT24134**
(4) CPU sends write address to **RTT24134**
(5) CPU verifies ACK signal from **RTT24134**
(6) CPU sends write data to the address specified at step (4)
(7) CPU verifies ACK signal from **RTT24134**
(8) Repeat (6) (7) if multiple bytes need to be written, address will be incremented automatically
(9) CPU ends stop condition[P]



3.3.2 Read Process

Writing the address to be read with write mode firstly, then reading the data with read mode.

(1) CPU sends start condition[S]
(2) CPU sends **RTT24134**'s slave address with R/W bit to set to write mode
(3) CPU verifies ACK signal from **RTT24134**
(4) CPU sends address for reading from **RTT24134**
(5) CPU verifies ACK signal from **RTT24134**
(6) CPU sends RESTART condition [Sr]
(7) CPU sends **RTT24134**'s slave address with R/W bit to set to read mode
(8) CPU verifies ACK signal from **RTT24134**
(9) CPU reads data from the specified address in step (4)
(10) CPU sends ACK signal for "0"
(11) Repeat (9) (10) if multiple bytes need to be read, address will be incremented automatically
(12) CPU sends ACK signal for "1"
(13) CPU sends stop condition[P]



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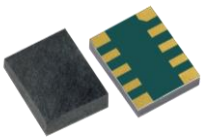


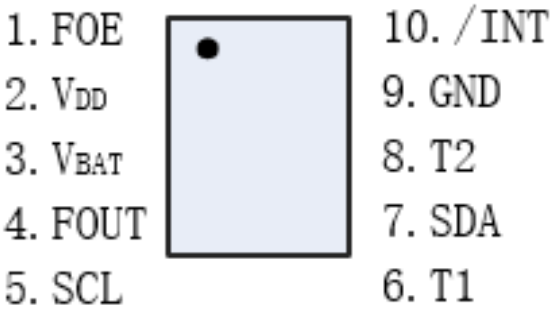
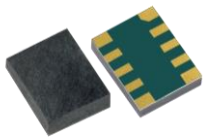
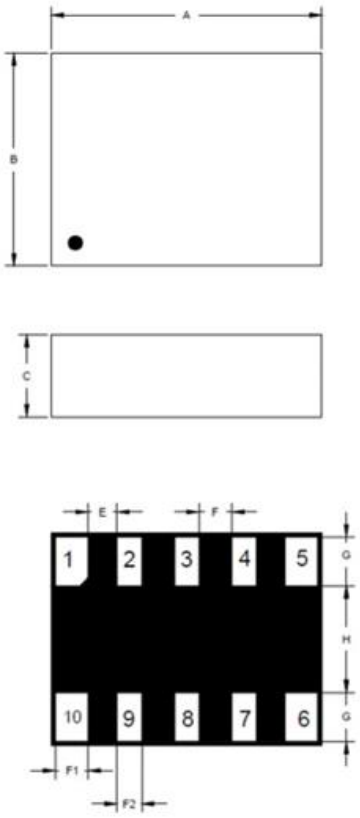


Table12. Pin Function

Pin Number	Pin Name	I/O	Description
1	FOE	In	FOUT output control pin. “1” - enable FOUT, “0”- FOUT Hi-Z
2	V_{DD}	-	Power supply
3	V_{BAT}	-	Backup battery pin. Connect to large-capacity capacitors or a backup battery. Connect to VDD when switchover function is not necessary.
4	FOUT	Out	Frequency output. Controlled by FOE. Frequency can be set by FSEL bits.
5	SCL	In	I^2C clock signal
6	T1	-	Manufacturer test only. Ensure to be floating
7	SDA	In/Out	I^2C data signal
8	T2	-	Manufacture test Only. Ensure to be floating
9	GND	-	Ground
10	/INT	Out	Interrupt Output, Open-Drain; Waveforms can be output in backup mode;

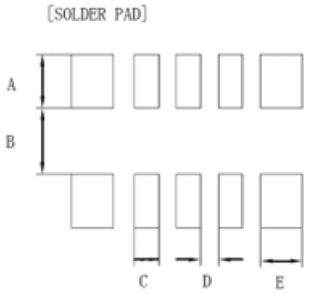
DIMENSIONS





Dimension	Min.	Typ.	Max.
A	3.0	3.2	3.4
B	2.3	2.5	2.7
C	--	1.0	--
D	--	0.3	--
E	--	0.4	--
F1	--	0.6	--
F2	--	1.3	--
G	--	0.45	--
H	--	0.3	--

Figure 2. Dimension

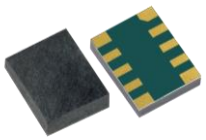


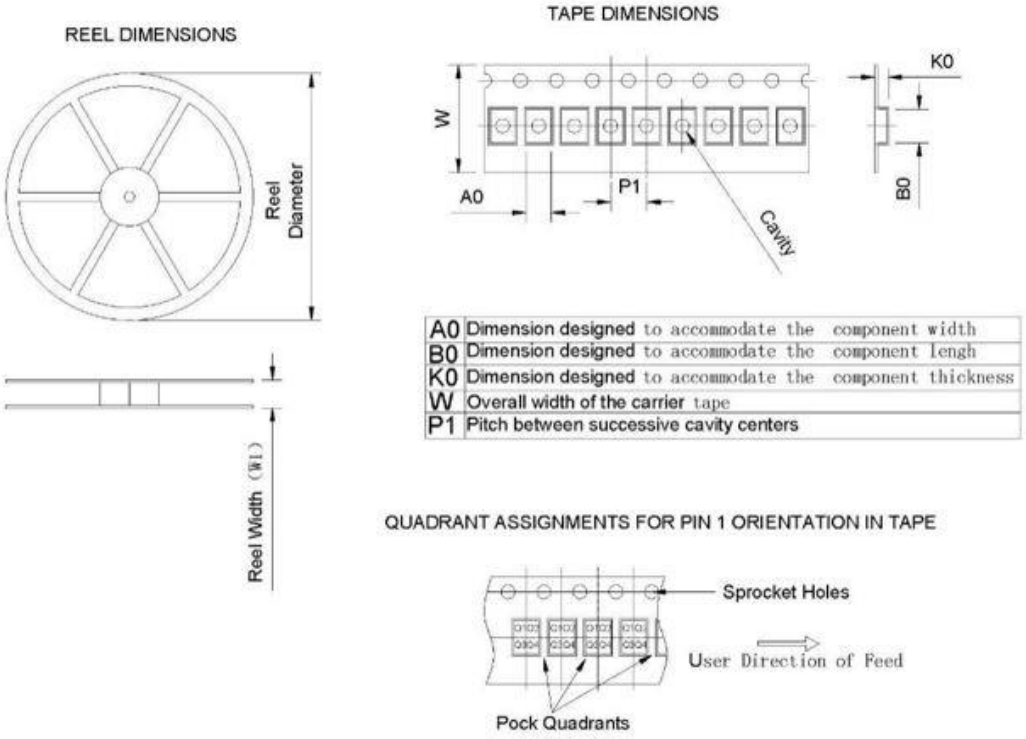
Dimension	Max.
A	0.9
B	1.1
C	0.4
D	0.3
E	0.7

(Unit: mm)

Figure 3. Recommended Soldering Pattern

PACKAGE

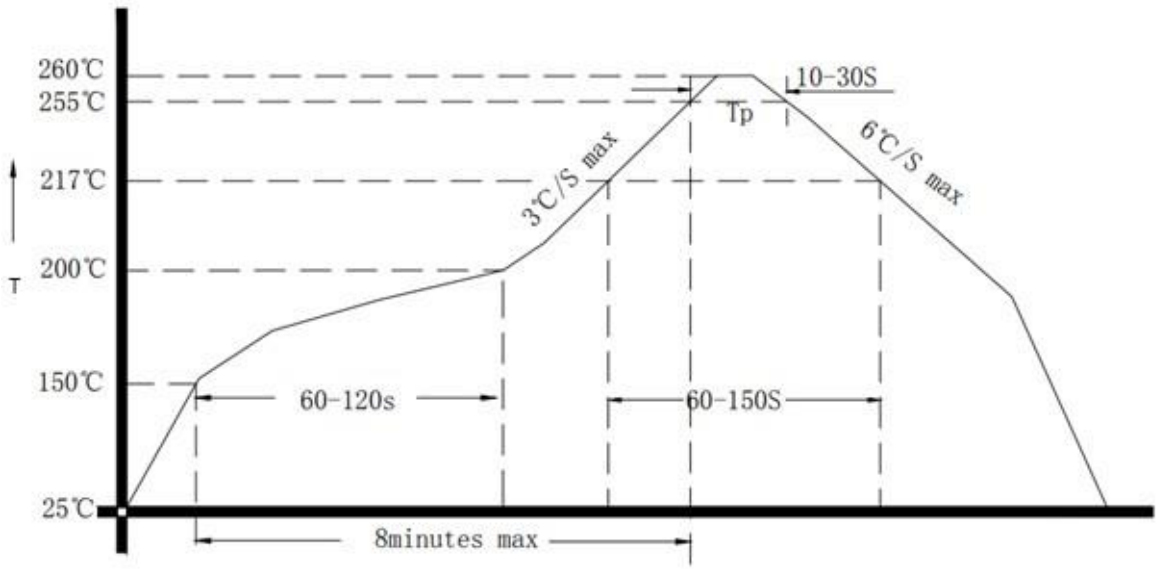




Pins	Reel Diameter (mm)	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
10	180	11.6±2.0	3.00	3.70	1.50	4.00	8.00

Figure 4. Package

REFLOW SOLDERING CURVE



Note: It is suggested to solder IC under the condition shown in the curve above. Must pay attention to the temperature and time when manual soldering, if the temperature over +260℃, or you will make the xo performance bad, even damage it.

APPROVAL

DRAWN BY:	AR, January 01, 2024
APPROVED BY:	CP, January 01, 2024
REVISION:	A, Initial Release
	B, AR, April 25, 2024 Updated the Current Revision Levels