MEMS MIC

RMIC-94-3.6-3526-RG-NS3

Features

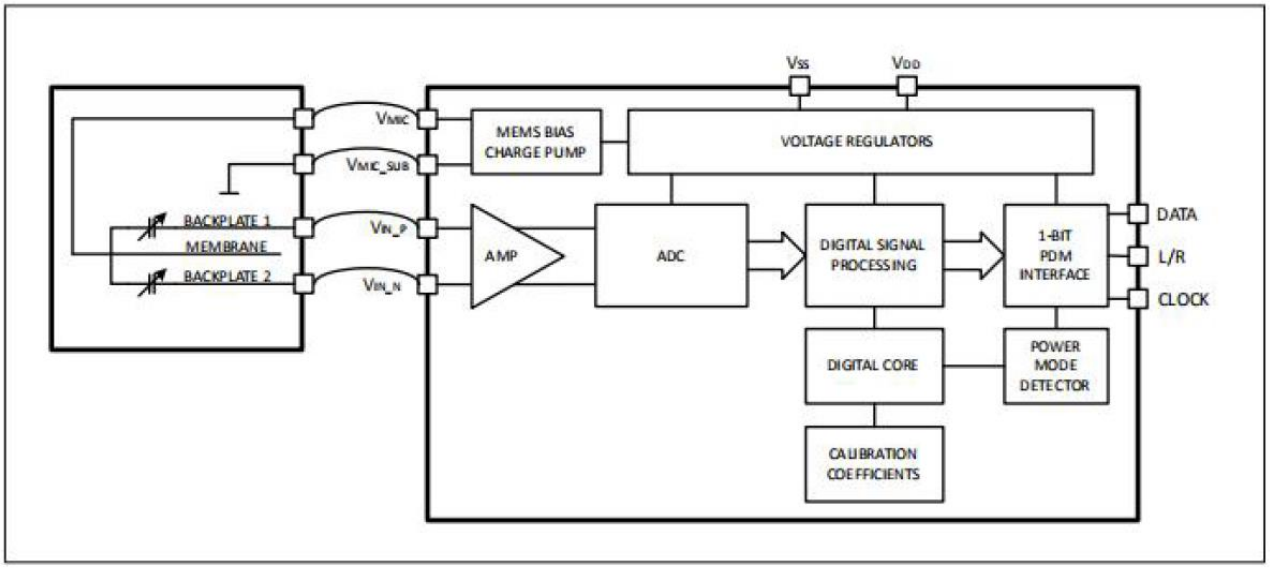
- 3.5x2.65x0.98mm Bottom Port
- PDM digital Output
- SNR of 66dBA
- RF Shielded
- Compatible with Standard SMD Reflow Technology
- RoHS Compliance & Halogen Free

Applications

- Smart Phones
- TWS Headsets
- Smart Speakers
- Wearable Electronics
- Portable Electronics
- Smart Home Electronics
- Laptop Computers

Description: RMIC-9403.6-3526-RG-NS3 is a digital MEMS microphone. The MEMS Microphones are integrated with specialized Pre-amplification ASIC to provide high sensitivity, high SNR output from a capacitive audio sensor. It's packaged for surface mounting and high temperature re-flow assembly.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Parameters	Value			Unit
	min	typ	max	
Supply Voltage			3.6	V
Supply Current			1	mA
Supply Current			1	mA
Operation Temperature Range	-40		+100	ºC
Storage Temperature Range	-40		+125	ºC

Note : Stresses at the maximum ratings shown in Table 1 may cause permanent damage to the device. These are stress ratings only at which the device may not function when an operation at these or any other condition beyond those specified under “Electro-Acoustic Specifications”.

ELECTRICAL SPECIFICATIONS

Test condition: Normal Mode: Vdd=1.8V, Fclk=3.072MHz, no load, unless otherwise specified.

Parameters		Value			Unit
		min	typ	max	
Directivity		Omni-Directional			
Clock Frequency (Fclk)		1.38	3.072	3.3	MHz
Sensitivity (S)	94db SPL@ 1kHz	-38	-37	-36	dBFS
Current Consumption (I)	Vdd=1.8V Fclk=3.072MHz		950	1300	uA
S/N Ratio (SNR)	94dB SPL @1kHz, A-Weighted		66		dBA
Total Harmonic Distortion (THD)	@ 94dB SPL @1kHz		0.02	0.5	%
	@ 115dB SPL @1kHz		0.03		
Acoustic Overload Point (AOP)	@1% THD @1kHz		129		dBSPL
	@10% THD @1kHz		132		
Power Supply Rejection (PSR)	@100mVpp Square wave, 217Hz, A-weighted		-99	-90	dBFS

Note: Frequency response, sensitivity, phase and current consumption are tested by 100% on product line.

Low Power mode (Vdd=1.8V, Fclk=768kHz, no load, unless otherwise specified)

Parameters		Value			Unit
		min	typ	max	
Clock Frequency (Fc)		450	768	850	kHz
Sensitivity (S)	@ 94db SPL@ 1kHz	-22	-21	-20	dBFS
Current Consumption (I)	@Vdd=1.8V, Fclk=768kHz		310	350	uA
S/N Ratio (SNR)	@ 94dB SPL @1kHz, A-Weighted		64.5		dBA
Total Harmonic Distortion (THD)	@ 94dB SPL @1kHz		0.3	0.5	%
Acoustic Overload Point (AOP)	@1% THD @1kHz		115		dB
Point	@10 THD @1kHz		116		dB
Power Supply Rejection (PSR)	@100mVpp Square wave, 217Hz, A-weighted		-94	-80	dB

Sleep Mode (Vdd=1.8V, Fclk=350 kHz)

Parameters		Value			Unit
		min	typ	max	
Clock Frequency (Fc)				350	kHz
Current Consumption (I)	Fclk=0kHz		1		uA
Current Consumption (I)	Fclk=350kHz		50		uA

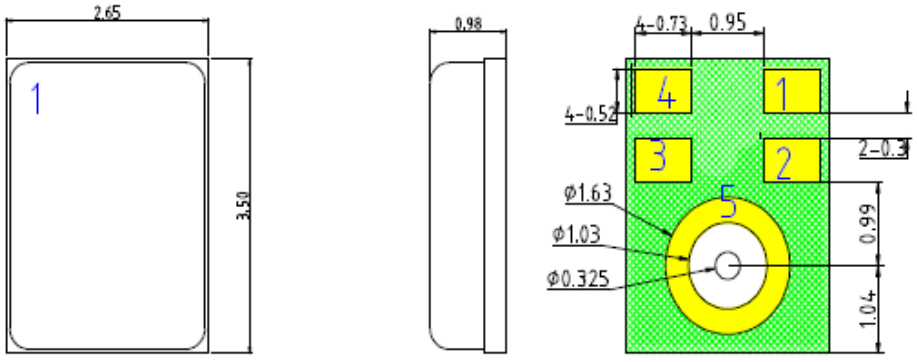
General Microphone Specification

Parameters		Value			Unit
		min	typ	max	
Supply Voltage	Vdd	1.62	1.8	3.6	V
Low Frequency Rolloff (LFRO)	-3dB relative to 1kHz		32		Hz
High Frequency Flatness	+3dB relative to 1 kHz		15		kHz
Polarity	Increasing sound pressure	Increasing density of 1' s			
Data Format		½ Cycle PDM			
Sensitivity Drop	Vdd(min)≤Vdd≤Vdd(max)	-0.5		0.5	dB
Short Output Current (Isc)	Data pin short to GND	1		20	mA
Output Load (Cload)				150	pF
Fall Asleep Time (Tslp)	Fclk<350kHZ			20	us
Wake-Up Time (Twk)	Fclk>350kHZ			20	ms
Power Up Time (Tpu)	Time to start up in any mode after Vdd off for >10ms Clock remain on			20	ms
Start Time	Time to start up in any mode after Vdd and clock applied			50	ms
Mode Change Time (Tmc)	Time to switch between modes			20	us

Digital interface electical specifications

Parameters		Value			Unit
		min	typ	max	
Input Logic Low Level	VIL	-0.3		0.35xVDD	V
Input Logic High Level	VIH	0.65xVDD			V
Output Logic Low Level	VOL			0.3xVDD	V
Output Logic High Level	VOH	0.7xVDD			V
Hysteresis Width	Vhyst	0.05xVDD			V
Clock Frequency	Fclk	0.35		3.3	MHz
Clock Duty Cycle	Fclock<=2.65MHz	45		55	%
	Fclock>=2.9MHzs	48		52	
Delay Time to Data Line Driven	Delay time from CLOCK edge (50% VDD) to DATA driven.	40		80	ns
Delay Time for DATA Valid	Delay time from CLOCK Edge (0.50 x VDD) to DATA valid (<0.30 x VDD or >0.70 x VDD)			100	ns
Delay time for DATA High-Z.	Delay time from CLOCK Edge (50% VDD) to DATA high impedance state.			30	ns
Clock Rise/Fall Time	Clock rise/fall time 35% to 65%			25	ns
DC Offset	LR=GND			-88	dBFS
	LR=VDD			-44	

DIMENSIONS

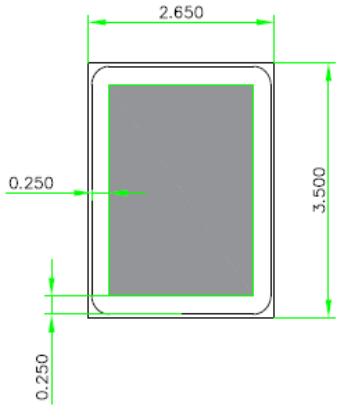


Top view Side view Bottom view

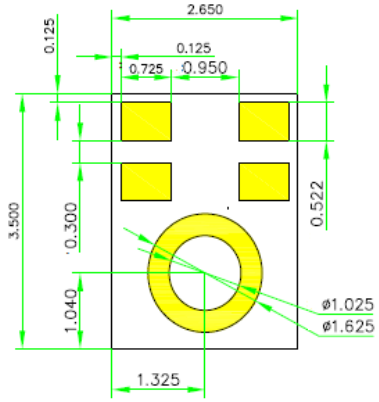
Unit: mm Unmarked Tolerance: ± 0.1 (mm)

Item	Dimension	Tolerance(+/-)	Units
Length(L)	3.50	0.10	mm
Width(W)	2.65	0.10	mm
Height(H)	0.98	0.10	mm
Acoustic Port(AP)	Ø0.325	0.05	mm

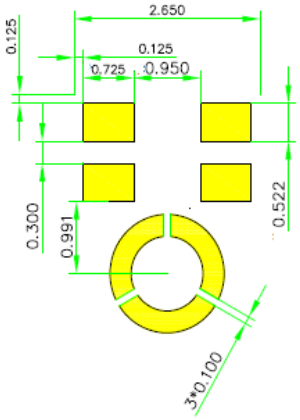
Pin No.	Pin Name	Type	Description
1	Data	Digital output	PDM output
2	L/R	L/R Channel	Channel select
3	CLK	Clock	Clock input
4	V_{DD}	Power	Power Supply
5	GND	Ground	Ground



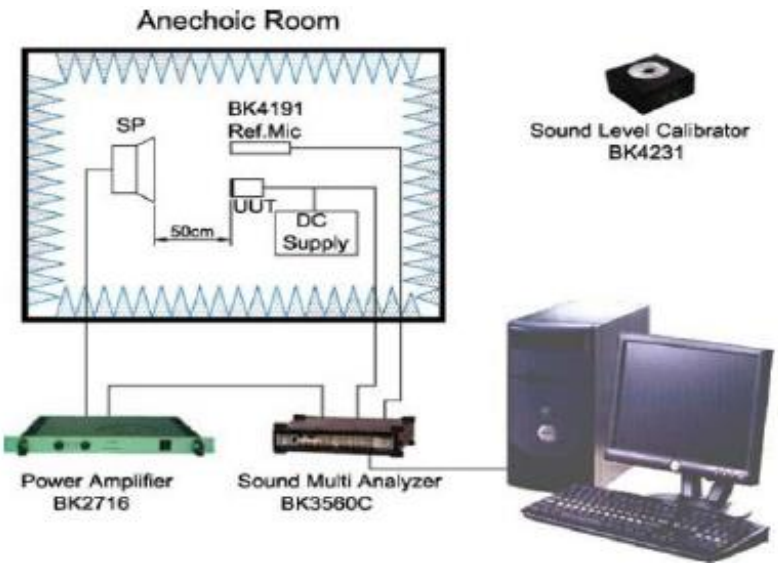
Pick up Area



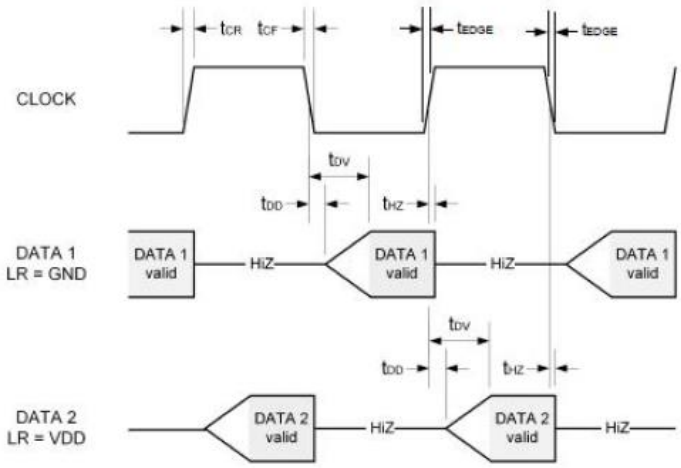
PCB Solder Land Pad



MEASUREMENT SYSTEM SETUP



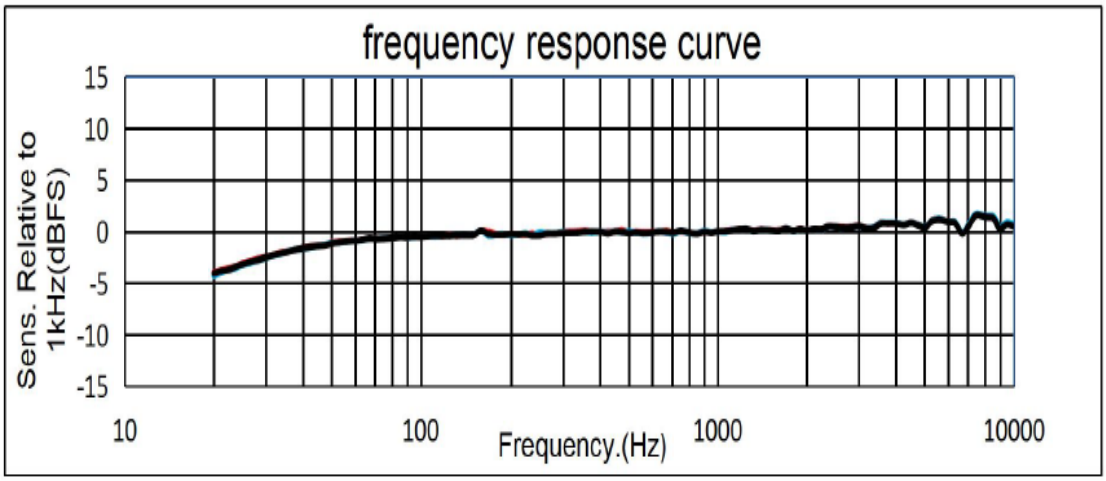
DIGITAL INTERFACE TIMING SPECIFICATION



PDM channel configuration using L/R pad

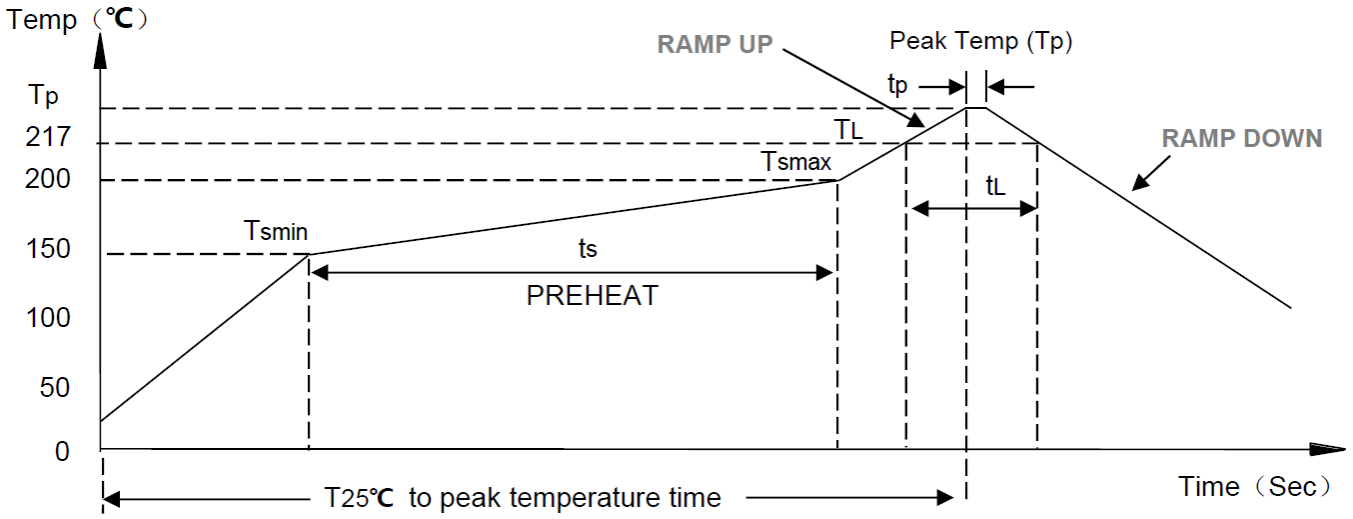
Channel	Data driven	Data high-Z	L/R connection
DATA1	Falling clock edge	Rising clock edge	GND
DATA2	Rising clock edge	Falling clock edge	VDD

FREQUENCY CHARACTERISTICS



Frequency(Hz)	LSL	USL	Unit
50	-3	1	dBFS
100	-2	1	dBFS
900	-1	1	dBFS
1000	0	0	dBFS
1100	-1	1	dBFS
3000	-1	3	dBFS
8000	-1	4	dBFS
10000	-1	6	dBFS

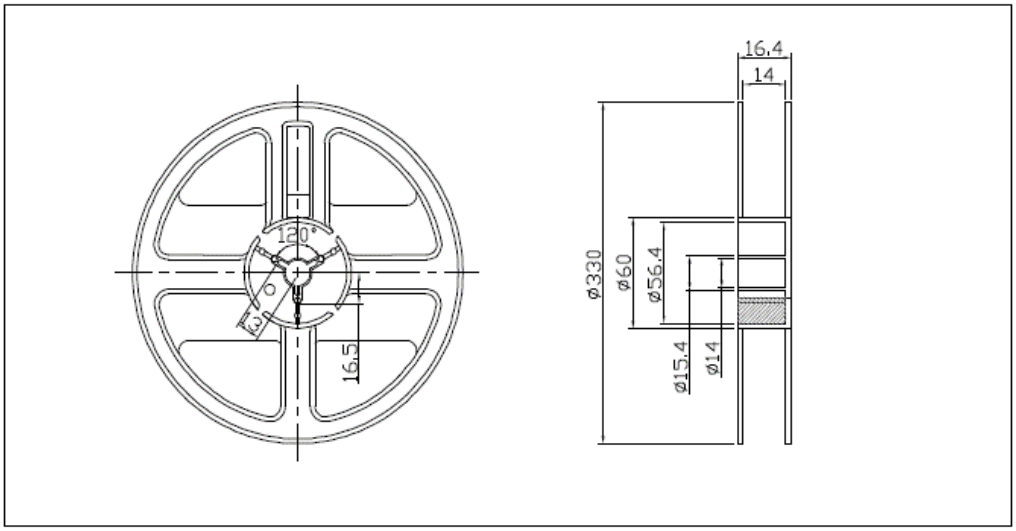
REFLOW PROFILE



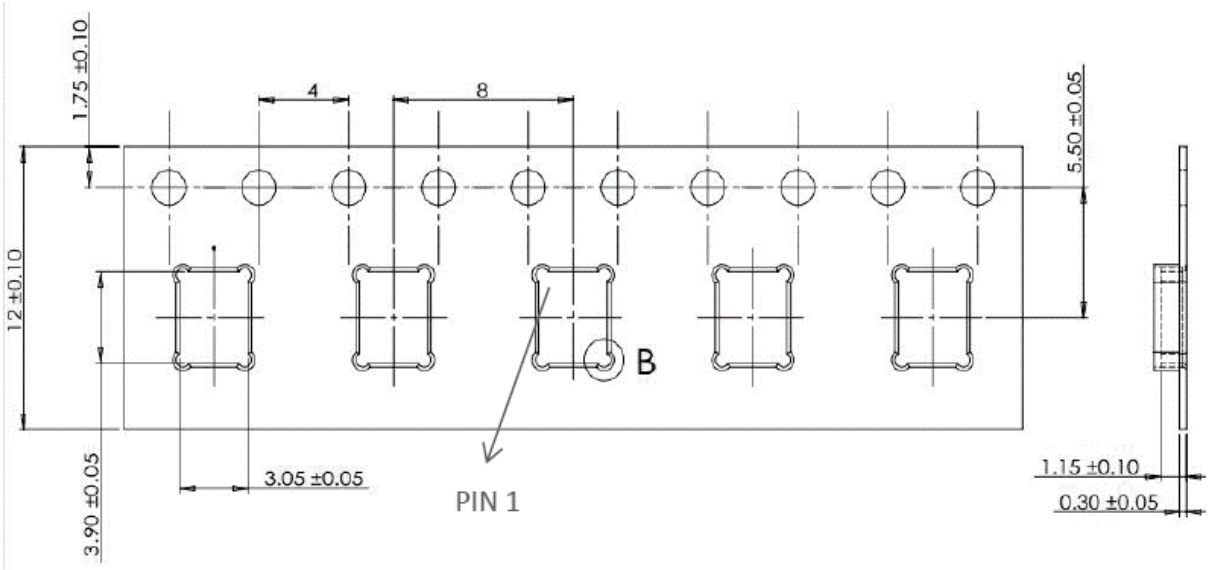
Parameter		Specification
Average temperature change rate (TSMAX to TP)		3°C /second max.
Preheat	Temperature min.(T_{SMIN})	150℃
	Temperature max.(T_{SMAX})	200℃
	Time T_{SMIN} to T_{SMAX}	60-180 Seconds
Time Maintained Above Liquidous		60-150 Seconds
Liquidous Temperature		217°C
Peak Temperature		260°C +0°C/−5°C
Time Within +5°C of Actual Peak Temperature		20 sec to 40 sec
Ramp-Down Rate		3°C/sec max
Time +25°C (t25°C) to Peak Temperature		8 min max

PACKAGING

13'' Reel drawing:



Tape drawing:



APPROVAL

DRAWN BY	AR, May 31, 2024
APPROVED BY	CP, May 31, 2024
REVISION	A, Initial Release