A RAMI TECHNOLOGY Company

HIGH FREQUENCY, LOW JITTER CLOCK OSCILLATOR

RoHS Compliant

OSCELOT

FAST TURNAROUND CLOCK OSCILLATOR

DESCRIPTION

The ***OSCELOT*** clock series is a cutting edge family of low to high frequency, **low jitter output**, **single** or **multi** - **frequency** clock oscillators. The ***OSCELOT*** clocks are available in **7.0 x 5.0, 5.0 x 3.2, and 3.2 x 2.5 mm** ceramic packages with output frequencies ranging from **10 MHz to 1.2 GHz.** Customer can select up to four output frequencies. Its outstanding flexibility significantly reduces design cycle time and overall cost. The ***OSCELOT*** clock design incorporates a low frequency crystal along with low jitter frequency synthesizer to provide a wide range of frequencies. The ***OSCELOT*** clocks are available in **LVCMOS**, **LVPECL** and **LVDS** outputs, allowing for a wide variety of applications. This product is ideal for the time conscious customer as shipments are made within days of a placed order.

FEATURES

- **Fast Turnaround (Ships Within Days)**
- **Very Low Jitter (Typical 0.6 ps)**
- **10 MHz to 1.2 GHz Frequency Range**
- **Selectable Single, Dual, or Quadruple Frequencies**
- **Stability as low as ±20 ppm (-40 ~ 85 °C)**
- **Available Sizes:**
  - ✓ **7.0 x 5.0 mm**
  - ✓ **5.0 x 3.2 mm**
  - ✓ **3.2 x 2.5 mm**

SELECTOR GUIDE	LVCMOS			LVDS			LVPECL		
Package Size (mm)	3.2x2.5	5.0x3.2	7.0x5.0	3.2x2.5	5.0x3.2	7.0x5.0	3.2x2.5	5.0x3.2	7.0x5.0
Family Part Number	HC3	HC5	HC7	LC3,MC3	LC5,MC5	LC7,MC7	PC3,QC3	PC5,QC5	PC7,QC7
Frequency Range (MHz)	10 – 250			10 – 1200			10 - 1200		
Frequency Stability (ppm)	±20, ±25, ±50, ±100			±20, ±25, ±50, ±100			±20, ±25, ±50, ±100		
Number of Frequencies	1,2,4			1,2,4			1,2,4		
Supply Voltage (V)	2.5, 3.3			2.5, 3.3			2.5, 3.3		
Temperature Range (°C)	-20 ~ +70			-20 ~ +70			-20 ~ +70		
	-40 ~ +85			-40 ~ +85			-40 ~ +85		
Enable/Disable Pin	Pin 1 or Pin 2			Pin 1or Pin 2			Pin 1or Pin 2		

RALTRON ELECTRONICS ▪ 10400 N.W. 33rd STREET ▪ Miami, Florida 33172 ▪ U.S.A.
Telephone: +1-305-593-6033 ▪ Fax: +1-305-594-3973 ▪ e-mail: sales@raltron.com ▪ web site: http://www.raltron.com

OUTPUT CHARACTERISTICS

	PARAMETER	SYMBOL	CONDITION		VALUE Min	VALUE Typ.	VALUE Max	UNIT
LVCMOS	Frequency Range	f_O			10		250	MHz
	Output Levels	V_{OH}			$0.9V_{cc}$			V
		V_{OL}					$0.1V_{cc}$	V
	Rise/Fall Time	T_r/T_f	20% - 80% (V_{OL}, V_{OH})				0.5	ns
	Supply Current	I_s	2.5V	10 – 50 MHz			25	mA
				51 – 135 MHz			35	
				136 – 180 MHz			37	
				180 -250 MHz			45	
			3.3V	10 – 50 MHz			35	
				51 – 135 MHz			50	
				136 – 250 MHz			60	
	Output Load	O_{CL}	Standard				15	pF

	PARAMETER	SYMBOL	CONDITION		VALUE Min	VALUE Typ.	VALUE Max	UNIT
LVPECL	Frequency Range	f_O			10		1200	MHz
	Output levels	V_{OH}	Load 50Ω to V_{cc}-2V		V_{cc}-1.03		V_{cc}-0.6	V
		V_{OL}			V_{cc}-1.85		V_{cc}-1.6	V
	Rise/Fall Time	T_r/T_f					0.25	ns
	Output Voltage Swing	V_{p-p}	Output termination 50Ω / V_{cc} - 2.0V		0.6		1.0	V
	Supply Current	I_s	2.5 V	10 – 50 MHz			35	mA
				51 – 215 MHz			45	
				216 – 640 MHz			65	
				641 – 1200 MHz			70	
			3.3V	10 – 50 MHz			85	
				51 – 215 MHz			95	
				216 – 640 MHz			115	
				641 – 1200 MHz			120	
	Output Load	O_{CL}	Output Termination 50Ω to V_{cc}-2V				50	Ω

	PARAMETER	SYMBOL	CONDITION		VALUE			UNIT
					Min	Typ.	Max	
LVDS	Frequency Range	f_O			10		1200	MHz
	Differential Output Voltage	V_{OD}	10 – 1200 MHz			0.6		V
	Offset Voltage	V_{OS}	V DC			1.3		V
	Rise/Fall Time	T_r/T_f					0.35	ns
	Supply Current	I_s	2.5V	10 – 50 MHz			25	mA
				51 – 215 MHz			30	
				216 – 640 MHz			43	
				641 – 1200 MHz			60	
			3.3V	10 – 50 MHz			65	
				51 – 215 MHz			72	
				216 – 640 MHz			83	
				641 – 1200 MHz			100	
	Output Load	O_{CL}	Differential 100Ω Load Connected Between Each Output				100	Ω

ELECTRICAL SPECIFICATIONS

PARAMETER		SYMBOL	CONDITION	VALUE			UNIT
				Min.	Typ.	Max.	
Supply Voltage[1]		V_{CC}			2.5 or 3.3		V
Duty Cycle		DC	Load depends on output type	45		55	%
RMS Phase Jitter		J	12 kHz – 20 MHz Bandwidth		0.6	1	ps
Overall Frequency Stability[1,2]		$\Delta f/f_c$	-10°C to +70°C			± 20 ± 25 ± 50	ppm
			-40°C to +85°C			± 25 ± 50 ±100	
Start-Up Time		t_{start}	T_a=25°C			10	ms
Enable		En	Min (logic 1 or open) HCMOS levels	$0.7V_{cc}$			V
Disable[3]		Dis	Max (logic 0) HCMOS levels			0.3	V
OE Function OE Pin Input LVCMOS/ LVTTL	Input Capacitance	C_{IN}			4		pF
	Input High Voltage	V_{IH}		$0.7V_{CC}$			V
	Input Low Voltage	V_{IL}				$0.3V_{CC}$	V
	Input High Current	I_{IH}				5	µA
	Input Low Current	I_{IL}		-10			µA
	Equivalent Internal Pull-up Resistance	R_{PULLUP}			900		kΩ
Aging			First year			±5	ppm
			Year thereafter			±2	
Operating Temperature [1]		T_a		-40		+85	°C
Storage Temperature		$T_{(stg)}$	Absolute max	-45		+100	°C
Absolute Voltage Range		$V_{cc(abs)}$				4.6	V
Moisture Sensitivity Level		MSL	JEDEC J-STD-020			1	
Termination Finish				Au			
ESD Sensitivity		HBM	Human body model JESD22-A114			3	kV

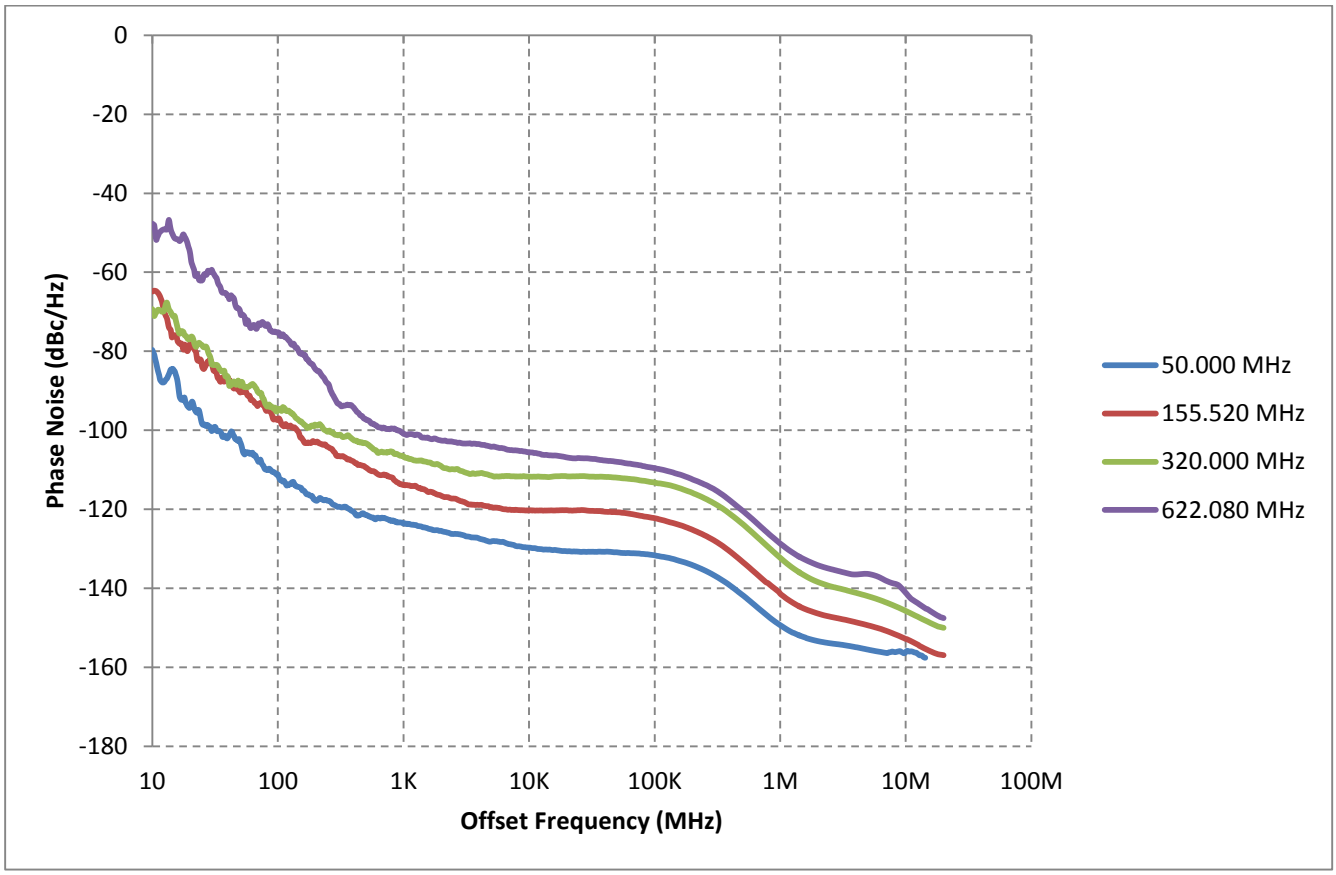
Notes

[1] See part numbering table

[2] Inclusive of 25°C calibration, tolerance, operating temperature range, input voltage variation, load change, aging, shock and vibration

[3] Output goes to high impedance

PHASE NOISE AND JITTER PERFORMANCE



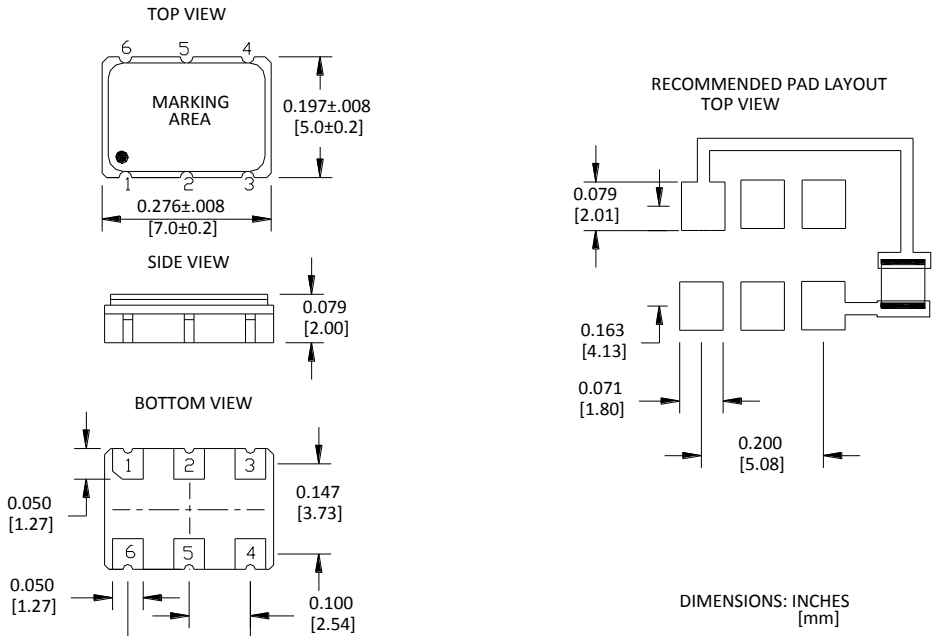
Data collected using Agilent E5052B signal source analyzer. V_{cc} = 2.5V.

FREQUENCY (MHz)	FULL BANDWIDTH PHASE JITTER (ps)	PHASE JITTER 12 kHz to 20 MHz INTEGRATED BANDWIDTH (ps RMS)
50.000	3.0	0.9
155.520	2.1	0.6
320.000	3.2	0.7
622.080	3.3	0.7

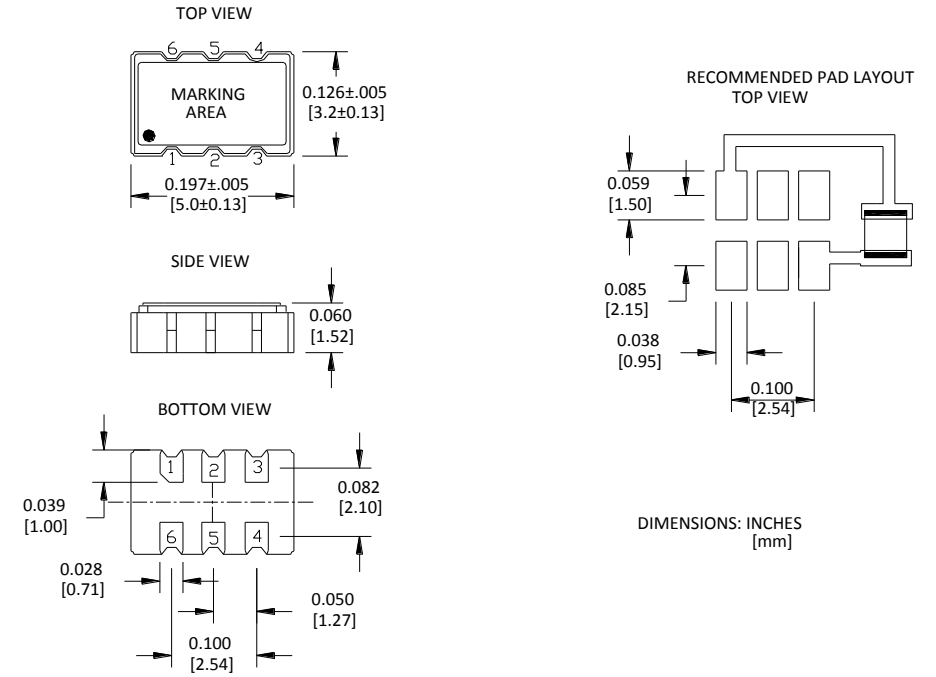
Phase jitter integrated using Agilent E5052B signal source analyzer. V_{CC} = 2.5V (LVCMOS, LVDS, LCPECL – load)

MECHANICAL DIMENSIONS AND PIN FUNCTIONING

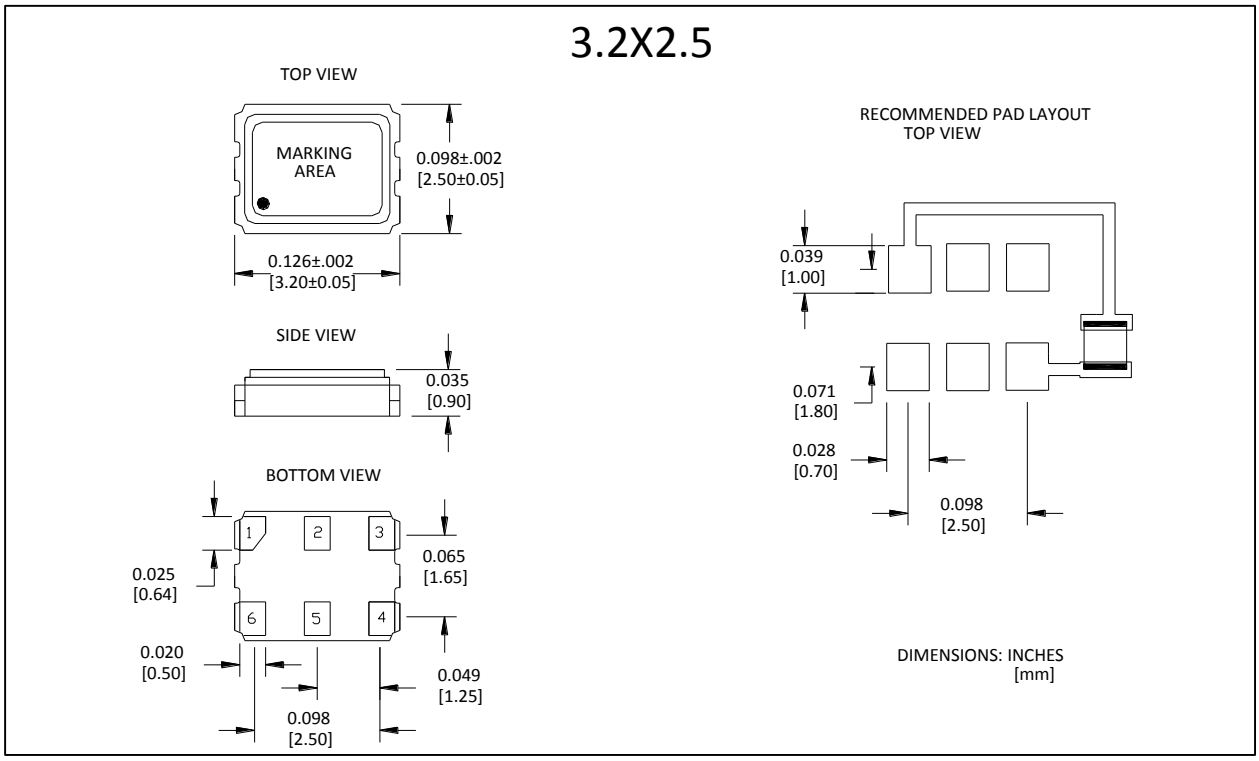
7.0X5.0



5.0X3.2



HIGH FREQUENCY, LOW JITTER CLOCK OSCILLATOR



Notes (Applicable To All Packages)

[1] Enable / Disable feature is available on either pin 1 or pin 2. See options on part numbering table.

[2] 0.01 µF external bypass capacitor is recommended as seen in solder pattern for 7 x 5 mm, and required for 5 x 3.2 and 3.2 x 2.5 mm

PIN	SYMBOL	FUNCTION
1	see below	Refer to Pin Logic Table Below
2	see below	Refer to Pin Logic Table Below
3	GND	Case and Electrical Ground
4	Output 1	Output 1
5	Output 2 or NC	Complementary Output (LVPECL, LVDS) or N/C (LVCMOS)
6	V_{cc}	Power Supply Voltage

PIN LOGIC TABLE			
NUMBER OF FREQUENCIES	PIN 1	PIN 2	FREQUENCY OUTPUT
1	Enable/Disable	N/C	F_1
	N/C	Enable/Disable	F_1
2	Enable/Disable	"0" Logic Level	F_1
		"1" Logic Level	F_2
	"0" Logic Level	Enable/Disable	F_1
	"1" Logic Level		F_2
4	"0" Logic Level	"0" Logic Level	F_1
	"0" Logic Level	"1" Logic Level	F_2
	"1" Logic Level	"0" Logic Level	F_3
	"1" Logic Level	"1" Logic Level	F_4

PART NUMBERING

SERIES	OUTPUT	SIZE (mm)	SUPPLY VOLTAGE (V)	FREQUENCY STABILITY (ppm)	TEMP RANGE (°C)	NUMBER OF FREQUENCIES	-	OUTPUT FREQUENCY (MHz)
ROSC	HC =CMOS LV =LVDS PC= LVPECL MC=LVDS, pin 2 E/D QC=LVPECL, pin2 E/D	**3=3.2x2.5** **5=5.0x3.2** **7=7.0x5.0**	**2**: V_{cc} = 2.5 **3**: V_{cc} = 3.3	**8:** ±20 **6I**: ±25 **5**: ±50 **0**: ±100	**blank**: -20~70 R: -40~85	**blank**: Single **2**: Dual **4**: Quad[1]	-	F_1 F_1 - F_2 F_1 - F_2 - F_3 - F_4

[1] There is no enable/disable option when the number of output frequencies is four. Enable/Disable pin option should be selected as 0.

EXAMPLE **ROSC HC 3 3 5 R 2 - 74.250 – 156.250**

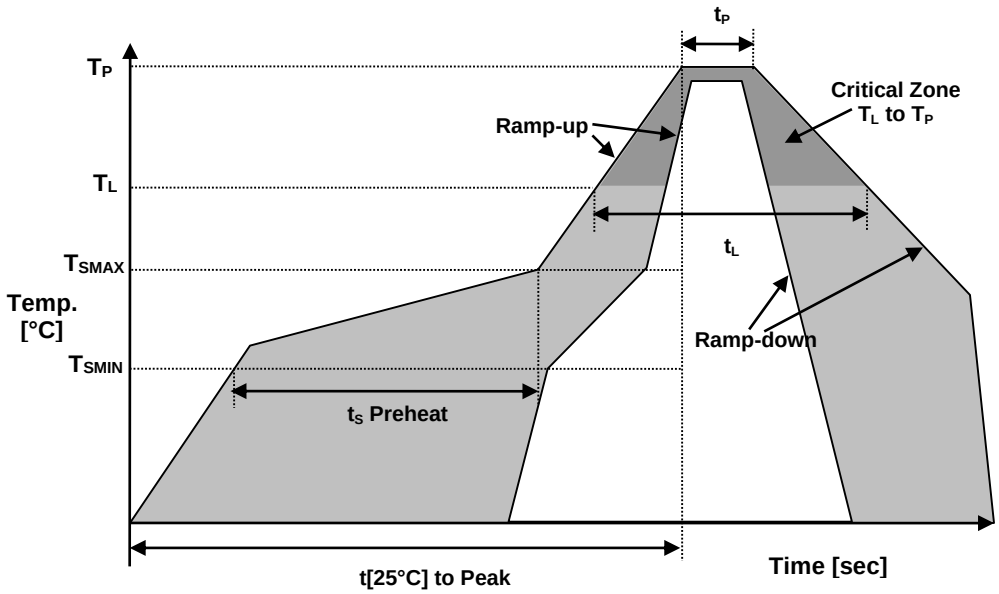
- OSCELOT Clock Oscillator
- HCMOS
- 3.2 x 2.5 mm
- 3.3 V
- ±50 ppm
- -40 ~ 85 °C
- Dual Frequency

- 1st Frequency: 74.250 MHz
- 2nd Frequency: 156.250 MHz

MARKING

- **A marking code will be issued by the sales department at order confirmation.**

REFLOW PROFILE



Recommended Solder Reflow Profile		
Temperature Min Preheat	T_{SMIN}	150°C
Temperature Max Preheat	T_{SMAX}	175°C
Time (T_{SMIN} to T_{SMAX})	t_S	60-180 sec.
Temperature	T_L	217°C
Peak Temperature	T_P	260°C
Ramp-up rate	R_{UP}	3°C/sec max.
Ramp-down rate	R_{DOWN}	6°C/sec max.
Time within 5°C of Peak Temperature	t_P	10 sec max.
Time t[25°C] to Peak Temperature	t[25°C] to Peak	480 sec.
Time	t_L	60-150 sec.

August 2015